

## Complete Publication List of Xiaobo Sharon Hu

### Book Chapters

1. T. Zhang\*, G. Tao, **X. Hu**, Q. Deng and S. Han, “Dynamic Resource Management in Real-Time Wireless Networks,” *Wireless Networks and Industrial IoT*, N.H. Mahmood, N. Marchenko, M. Gidlund, P. Popovski (Eds.), Springer, 2021, pp. 131–156.
2. Y. Ma\*, J. Zhou, T. Chantem\*, R. P. Dick, and **X. Hu**, “Resource Management for Improving Overall Reliability of Multi-Processor Systems-on-Chip,” *Dependable Embedded Systems*, J. Henkel and N. Dutt (Eds.), Springer International Publishing, 2021, pp. 233–246.
3. Y Bi, P.-E. Gaillardon, **X. Hu**, M. Niemier, J.-S. Yuan and Y. Jin, “Polarity-Controllable Silicon NanoWire FET-Based Security,” *Security Opportunities in Nano Devices and Emerging Technologies*, M. Tehranipoor, D. Forte, G.S. Rose, S. Bhunia (Eds.), Taylor & Francis, 2017, pp. 165–178.
4. G.Csaba, G.H. Bernstein, A. Orlov, M.T. Niemier, **X. Hu** and W.Porod, “Nanomagnetic logic: from magnetic ordering to magnetic computing,” *CMOS and Beyond: Logic Switches for Terascale Integrated Circuits*, T.-J.K. Liu, K.J. Kuhn (Eds.), Cambridge University Press, 2015, pp. 301–334.
5. W.Porod, G.H. Bernstein, G.Csaba, **X. Hu**, J.J. Nahas, M.T. Niemier and A. Orlov, “Nanomagnet Logic (NML),” *Field-Coupled Nanocomputing*, N.G. Anderson and S. Bhanja (Eds.), Springer, 2014, pp. 21–32.
6. R.F. Barrett, S. Borkar, S.S. Dosanjh, S.D. Hammond, M.A. Heroux, **X. Hu**, J. Luitjens, S.G. Parker, J. Shalf and L. Tang, “On the Role of Co-design in High Performance Computing,” *Transition of HPC Towards Exascale Computing*, E.H. D’Hollander, J.J. Dongarra, I. Foster, L. Grandinetti and G.R. Joubert (Eds.), IOS Press, November 2013, pp 141–155.
7. Y. Zhang\*, **X. Hu** and D.Z. Chen, “Energy Minimization in Multiprocessor Real-Time Systems,” *Handbook of Energy-Aware and Green Computing*, I. Ahmad and S. Ranka (Eds.), CRC Press, January 2012, pp 519–542.
8. G. Quan\* and **X. Hu**, “Minimum Energy Fixed-Priority Scheduling for Variable Voltage Processors,” *Design, Automation, and Test in Europe – The Most Influential Papers of 10 Years DATE*, R. Lauwereins and J. Madsen (Eds.), Springer, March 2008, pp. 313–324.
9. **X. Hu** and G. Quan\*, “Fundamentals of Power-Aware Scheduling,” *Embedded Processor and System Design – A Low Power Perspective*, J. Henkel and S. Parameswaran (Eds.), Kluwer Academic Publishers, 2007, pp. 219–229.
10. G. Quan\* and **X. Hu**, “Static DVFS Scheduling,” *Embedded Processor and System Design – A Low Power Perspective*, J. Henkel and S. Parameswaran (Eds.), Kluwer Academic Publishers, 2007, pp. 231-242.

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Student or postdoctoral fellow advised or co-advised by X. Sharon Hu.

11. G.W. Greenwood, **X. Hu** and J.G. D’Ambrosio, “Fitness functions for multiple objective optimization problems: Combining preferences with Pareto rankings,” *Foundations of Genetic Algorithms*, R. Belew and M. Vose (Eds.), Morgan-Kaufmann, 1997, pp. 437–455.

### Refereed Journal Articles (published or accepted for publication)

1. S. Mishra\*, D.Z. Chen and **X. Hu**, “Data-driven Deep supervision for medical image segmentation,” accepted to *IEEE Transactions on Medical Imaging (IEEE TMI)*, 2022.
2. A. Kazemi\*, M. M. Sharifi\*, A. F. Laguna\*, F. Müller, X. Yin, T. Kämpfe, M. Niemier and **X. Hu**, “FeFET multi-bit content-addressable memories for in-memory nearest neighbor search,” accepted to *IEEE Transactions on Computers (IEEE TC)*, 2021.
3. L. Zhang, S. Mishra\*, T. Zhang\*, Y. Zhang, D. Zhang, Y. Lv, M. Lv, N. Guan, **X. Hu**, D. Z. Chen and X. Han, “Design and assessment of convolutional neural network based methods for vitiligo diagnosis,” accepted to *Frontiers in Medicine, section Dermatology*, 2021.
4. Q. Huang, D. Reis\*, C. Li, D. Gao, M. T. Niemier, **X. Hu**, M. Imani, X. Yin and C. Zhuo, “Computing-in-memory using ferroelectrics: from single- to multi-input logic,” accepted to the Special Issue on Near-Memory and In-Memory Processing, *IEEE Design & Test of Computers*, 2021.
5. S. Mishra\*, D. Z. Chen and **X. Hu**, “Image complexity guided network compression for biomedical image segmentation,” *ACM Journal on Emerging Technologies in Computing Systems (ACM JETC)*, Vol. 18, No. 2, Article 26, 2021, pp. 1–23.
6. S. Mishra\*, Y. Wang, C. Wei, D. Z. Chen and **X. Hu**, “VTG-Net: A CNN based vessel topology graph network for retinal artery/vein classification,” *Frontiers in Medicine*, Vol. 8, 2021, pp. 2124 (10 pages).
7. D. Reis\*, M. T. Niemier and **X. Hu**, “The implications of ferroelectric FET device models to the design of computing-in-memory architectures,” Special Issue on Future Trends in Nanocomputing, *Journal of Integrated Circuits and Systems*, Vol. 16, No. 1, 2021, pp. 1–8.
8. T. Zhang\*, T. Gong, S. Han, Q. Deng and **X. Hu**, “Fully distributed packet scheduling framework for handling disturbances in lossy real-time wireless networks,” *IEEE Transactions on Mobile Computing (IEEE TMC)*, Vol. 20, No. 2, 2021, pp. 502–518.
9. B. Wu\*, Z. Wang, Y. Li, Y. Wang, D. Liu, W. Zhao and **X. Hu**, “A NAND-SPIN based magnetic ADC,” *IEEE Transactions on Circuits and Systems II: Express Briefs (IEEE TCAS II)*, Vol. 68, No. 2, 2021, pp. 617–621.
10. X. Xu, X. Zhang, B. Yu, **X. Hu**, C. Rowen, J. Hu and Y. Shi, “DAC-SDC low power object detection challenge for UAV applications,” *IEEE Transactions on Pattern Analysis and Machine Intelligence (IEEE PAMI)*, Vol. 43, No. 2, 2021, pp. 392–403.
11. R. Rajaei\*, M. M. Sharifi\*, A. Kazemi\*, M. Niemier and **X. Hu**, “Compact single-phase-search multi-state content addressable memory design using 1 FeFET/cell,” *IEEE Transactions on Electron Devices (IEEE TED)*, Vol. 68, No. 1, 2021, pp. 109–117.

12. Y. Xi, H. Wu, B. Gao, J. Tang, A. Chen, M.-F. Chang, **X. Hu**, J. Van der Spiegel and H. Qian, “In-memory learning with analog resistive switching memory: a review and perspective,” *Proceedings of the IEEE*, Vol. 109, No. 1, 2021, pp. 14–42.
13. P. Wu, D. Reis\*, **X. Hu** and J. Appenzeller, “Two-dimensional transistors with reconfigurable polarities for secure circuits,” *Nature Electronics*, Vol. 4, 2021, pp. 45–53.
14. L. Li, J. Zhou\*, M. Chen, T. Wei and **X. Hu**, “Learning-based modeling and optimization for real-time system availability,” Special Issue on Machine-Learning Architectures and Accelerators, *IEEE Transactions on Computers (IEEE TC)*, Vol. 70, No. 4, 2020, pp. 581–594.
15. W. Jiang, Q. Lou\*, Z. Yan\*, L. Yang, J. Hu, **X. Hu** and Y. Shi “Device-circuit-architecture co-exploration for computing-in-memory neural accelerators,” *IEEE Transactions on Computers (IEEE TC)*, Vol. 70, No. 4, 2020, pp. 595–605.
16. D. Gao, D. Reis\*, **X. Hu** and C. Zhuo, “Eva-CiM: a system-level performance and energy evaluation framework for computing-in-memory architectures,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 39, No. 12, pp. 5011–5024, 2020.
17. Y. Ding, W. Jiang, Q. Lou\*, J. Liu, J. Xiong, **X. Hu**, X. Xu, and Y. Shi, “Hardware design and the competency awareness of a neural network,” *Nature Electronics*, Vol. 3, 2020, pp. 514–523.
18. F. Molnàr, S.R. Kharel, **X. Hu** and Z. Toroczkai, “Accelerating a continuous-time analog SAT solver using GPUs,” *Computer Physics Communications*, Vol. 256, 2020, 107469.
19. D.Y. Zhang, Y. Ma\*, **X. Hu** and D. Wang, “Towards privacy-aware task allocation in social sensing based edge computing systems,” *IEEE Internet of Things Journal (IEEE IoT-J)*, Vol. 7, No. 12, 2020, pp. 11384–11400.
20. B. Wu\*, C. Wang, Z. Wang, Y. Wang, D. Zhang, D. Liu, Y. Zhang and **X. Hu**, “Field-free 3T2SOT MRAM for non-volatile cache memories,” *IEEE Transactions on Circuits and Systems I (IEEE TCAS I)*, Vol. 67, No. 12, 2020, pp. 4660–4669.
21. D. Reis\*, J. Takeshita, T. Jung, M. Niemier and **X. Hu**, “Computing-in-Memory for performance and energy efficient homomorphic encryption,” *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 28, No. 11, 2020, pp. 2300–2313.
22. H. Wang , N. C. Audsley , **X. Hu** and W. Chang, “Meshed Bluetree: Time-predictable multi-memory interconnect for multi-core architectures,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 39, No. 11, 2020, pp. 3787-3798.
23. Y. Ma\*, J. Zhou\*, T. Chantem\*, R. Dick, S. Wang and **X. Hu**, “Improving reliability of real-time embedded systems on integrated CPU and GPU platforms,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 39, No. 10, 2020, pp. 2218-2229.

24. M. Imani, X. Yin\*, J. Messerly, S. Gupta, M. Nemier, **X. Hu** and T. Rosing, "SearchHD: A memory-centric hyperdimensional computing with stochastic training," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 39, No. 10, 2020, pp. 2422-2433.
25. C. Leng, Y. Qiao, **X. Hu** and H. Wang, "Co-Scheduling aperiodic real-time tasks with end-to-end firm and soft deadlines in two-stage systems," *Real-Time Systems (RTS)*, Vol. 56, 2020, pp. 56, 391-451.
26. Y. Ding, W. Jiang, Q. Lou\*, J. Liu, J. Xiong, **X. Hu**, X. Xu, and Y. Shi, "Hardware design and the competency awareness of a neural network," *Nature Electronics*, Vol. 3, 2020, pp. 514-523.
27. B. Wu\*, P. Dai, Z. Wang, C. Wang, Y. Wang, J. Yang, Y. Cheng, D. Liu, Y. Zhang, W. Zhao and **X. Hu**, "Bulkyflip: A NAND-SPIN based last-level cache with bandwidth-oriented write management policy," *IEEE Transactions on Circuits and Systems I: Regular Papers (IEEE TCAS I)*, Vol. 67, No. 1, 2020, pp. 108-120.
28. X. Chen\*, S. Datta, **X. Hu**, M. Jerry, A. Laguna\*, K. Ni, M. Niemier, D. Reis\*, X. Sun, P. Wang, X. Yin\* and S. Yu, "The impact of ferroelectric FETs on digital and analog circuits and architectures," *IEEE Design & Test*, Vol. 37, No. 1, 2020, pp. 79-99.
29. X. Yin\*, C. Li, Q. Huang, L. Zhang, M. Niemier, **X. Hu**, C. Zhuo and K. Ni, "FeCAM: A universal compact digital and analog content addressable memory using ferroelectric," *IEEE Transactions on Electron Devices (IEEE TED)*, Vol. 67, No. 7, 2020, pp. 2785-2792.
30. J. Chen, H. Wu, B. Gao, J. Tang, **X. Hu** and H. Qian, "A parallel multi-bit programming scheme with high precision for RRAM-based neuromorphic systems," *IEEE Transactions on Electron Devices (IEEE TED)*, Vol. 67, No. 5, 2020, pp. 2213-2217.
31. Y. Ma\*, J. Zhou, T. Chantem\*, R. Dick, S. Wang and **X. Hu**, "On-line resource management for improving reliability of real-time systems on "Big-Little" type MPSoCs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 39, No. 1, 2020, pp. 88-100.
32. T. Zhang\*, T. Gong, S. Han, Q. Deng and **X. Hu**, "Distributed dynamic packet scheduling framework for handling disturbances in real-time wireless networks," *IEEE Transactions on Mobile Computing (IEEE TMC)*, Vol. 18, No. 11, 2019, pp. 2502-2517.
33. C. Pan, Q. Lou\*, M. Niemier, **X. Hu** and A. Naeemi, "Energy-efficient convolutional neural network based on cellular neural network using beyond-CMOS technologies," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (IEEE JxCDC)*, Vol. 5, No. 2, 2019, pp. 85-93.
34. J. Zhou\*, X. Zhou, J. Sun, T. Wei, M. Chen, S. Hu and **X. Hu**, "Resource management for improving soft-error and lifetime reliability of real-time MPSoCs" *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 38, No. 12, 2019, pp. 2215-2228.

35. D. Reis\*, M. Niemier and **X. Hu**, “A computing-in-memory engine for searching on homomorphically encrypted data,” *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (IEEE JxCDC)*, Vol. 5, No. 2, 2019, pp. 123–131.
36. D. Reis\*, K. Ni, W. Chakraborty, X. Yin\*, M. Trentzsch, S. Dünkel, J. Müller, S. Beyer, S. Datta, M. Niemier and **X. Hu**, “Design and analysis of an ultra-dense, low-leakage and fast FeFET-based random access memory array,” *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (IEEE JxCDC)*, Vol. 5, No. 2, 2019, pp. 103–112.
37. A. Stephan, Q. Lou\*, M. Niemier, **X. Hu** and S. Koester, “Nonvolatile spintronic memory cells for neural networks,” *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (IEEE JxCDC)*, Vol. 5, No. 2, 2019, pp. 67–73.
38. K. Ni, X. Yin\*, A. Laguna\*, S. Joshi, S. Dünkel, M. Trentzsch, J. Müller, S. Beyer, W. Taylor, M. Niemier, **X. Hu** and S. Datta, “Ferroelectric ternary content addressable memory for one-shot learning,” *Nature Electronics*, Vol. 2, No. 11, 2019, pp 521–529.
39. A. Chen, S. Datta, **X. Hu**, M. Niemier, T. Simunic Rosing and J. J. Yang, “A survey on architecture advances enabled by emerging beyond-CMOS technologies,” *IEEE Design & Test*, Vol. 36, No. 3, 2019, pp. 46–68.
40. J. Zhou\*, **X. Hu**, Y. Ma\*, J. Sun, T. Wei and S. Hu, “Improving availability of multicore real-time systems suffering both permanent and transient faults,” *IEEE Transactions on Computers (IEEE TC)*, Vol.68, No. 12, 2019, pp. 1785–1801.
41. Q. Lou\*, C. Pan, J. Mcguinness, A. Horvath, A. Naeemi, M Niemier and **X. Hu**, “A mixed signal architecture for convolutional neural networks,” *ACM Journal on Emerging Technologies in Computing Systems (ACM JETC)*, Vo. 15, No. 2, 2019, Article No. 19.
42. X. Yin\*, K. Ni, D. Reis, S. Datta, M. Niemier and **X. Hu**, “An ultra-dense 2FeFET TCAM design based on a multi-domain FeFET model,” *IEEE Transactions on Circuits and Systems II: Express Briefs (IEEE TCAS II)*, Vol. 66, No. 9, 2019, pp. 1577–1581.
43. X. Chen\*, D. Chen, Y. Han and **X. Hu**, “moDNN: Memory optimal deep neural network training on Graphics Processing Units,” *IEEE Transactions on Parallel and Distributed Systems (IEEE TPDS)*, Vol. 30, No. 3, 2019, pp. 646–661.
44. X. Yin\*, X. Chen\*, M. Niemier and **X. Hu**, “Ferroelectric FETs based nonvolatile logic-in-memory circuits,” *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 27, No. 1, 2019, pp. 159–172.
45. L. Li, P. Cong, K. Cao, J. Zhou\*, T. Wei, M. Chen, S. Hu and **X. Hu**, “Game theoretic feedback control for reliability enhancement of EtherCAT-based networked systems,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 38, No. 9, 2019, pp. 1599–1610.
46. K. Cao, J. Zhou\*, T. Wei, M. Chen, S. Hu and **X. Hu**, “Affinity-driven modeling and task scheduling for makespan optimization in heterogeneous multiprocessor systems considering reliability and temperature,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 38, No. 7, 2019, pp. 1189–1202.

47. X. Chen\*, K. Ni, M. Niemier, Y. Han, S. Datta and **X. Hu**, “Power and area efficient FPGA building blocks based on ferroelectric FETs,” *IEEE Transactions on Circuits and Systems I: Regular Papers (IEEE TCAS I)*, Vol. 66, No. 5, 2019, pp. 1780–1793.
48. **X. Hu** and M. Niemier, “Cross-layer efforts for energy-efficient computing—Towards peta operations per second per watt,” *Frontiers of Information Technology & Electronic Engineering*, Vol. 19, No. 10, 2018, pp. 1209–1223.
49. M. Jerry, S. Dutta, A. Kazemi, K. Ni, J. Zhang, P.-Y. Chen, P. Sharma, S. Yu, **X. Hu**, M. Niemier and S. Datta, “A ferroelectric field effect transistor based synaptic weight cell,” *Journal of Physics D: Applied Physics*, Vol. 51, No. 43, 2018, pp. 434001.
50. R. Perricone\*, **X. Hu**, J. Nahas, and M. Niemier, “Can beyond CMOS devices illuminate dark silicon,” *Communications of the ACM (CACM) (ACM CACM)*, Vol. 61, No. 9, 2018, pp. 60–69.
51. T. Wei, J. Zhou, K. Cao, P. Cong, M. Chen, G. Zhang, **X. Hu** and J. Yan, “Cost-constrained QoS optimization for approximate computation real-time tasks in heterogeneous MPSoCs,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 37, No. 9, 2018, pp. 1733–1746.
52. X. Yin\*, B. Sedighi, M. Varga, M. Ercsey-Ravasz, Z. Toroczkai and **X. Hu**, “Efficient analog circuits for Boolean satisfiability,” *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 26, No. 1, 2018, pp. 155–167.
53. X. Xu, Y. Ding, **X. Hu**, M. Niemier, J. Cong, Y. Hu and Y. Shi, “Scaling for edge inference of deep neural networks,” *Nature Electronics*, Vol. 1, No. 4, 2018, pp. 216–222.
54. T. Wu, Y. Liu, D. Zhang, J. Li, **X. Hu**, C. J. Xue and H. Yang. “DVFS based long-term task scheduling for dual-channel solar-powered sensor nodes,” *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 25, No. 11, 2017, pp. 2981–2994.
55. Y. Ma\*, T. Chantem\*, R.P. Dick and **X. Hu**, “Improving system-level lifetime reliability of multicore soft real-time systems,” *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 25, No. 6, 2017, pp. 1895–1905.
56. Y. Bi, K. Shamsi, J. Yuan, Y. Jin, M.T. Niemier and **X. Hu**, “Tunnel FET current mode logic for DPA resilient circuit designs,” *IEEE Transactions on Emerging Topics in Computing (IEEE TETC)*, Vol. 5, No. 3, 2017, pp. 340–352.
57. L. Tang\*, **X. Hu**, R. Barrett and J. Cook, “PeaPaw: Performance and energy aware partitioning of workload on heterogeneous platforms,” *ACM Transactions on Design Automation of Electronic Systems (ACM TODAES)*, Vol. 22, No. 3, 2017, pp. 41:1–41:26.
58. J. Fernandez-Berni, M. Niemier, **X. Hu**, H. Lu, W. Li, P. Fay, R. Carmona-Galan and A. Rodriguez-Vazquez, “TFET-based well capacity adjustment in active pixel sensor for enhanced high dynamic range,” *Electronic Letters*, Vol. 53, No. 9, 2017, pp. 622–624.
59. T. Liu, H. Guo, S. Parameswaran and **X. Hu**, “iCETD: An improved tag generation design for memory data authentication in embedded processor systems,” *Integration, the VLSI Journal*, Vol. 56, pp. 96–104, 2017.

60. Y. Bi, K. Shamsi, P.E. Gaillardon, G.de Micheli, X. Yin\*, **X. Hu**, M.T. Niemier, J. Yuan and Y. Jin, “Emerging technology based design of primitives for hardware security,” *ACM Journal on Emerging Technologies in Computing (ACM JETC)*, Vo. 13, No. 1, 2016, pp. 3:1–3:19.
61. J. Zhou\*, T. Wei, M. Chen, J. Yan, **X. Hu** and Y. Ma\*, “Thermal-aware task scheduling for energy minimization in heterogeneous real-time MPSoC systems,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 35, No. 8, 2016, pp. 1269–1282.
62. D. Zhang, S. Li, Y. Liu, **X. Hu**, X. He, Y. Zhang, P. Zhang and H. Yang, “A C2RTL framework supporting partition, parallelization, and FIFO sizing for streaming applications,” *ACM Transactions on Design Automation of Electronic Systems (ACM TODAES)*, Vol. 21, No. 2, 2016, pp. 19:1–19:32.
63. R. Perricone\*, Y. Liu\*, A. Dingler\*, **X. Hu** and Michael Niemier, “Design of stochastic computing circuits using nanomagnetic logic,” *IEEE Transactions on Nanotechnology (IEEE TNANO)*, Vol. 15, No. 2, 2016, pp. 179–187.
64. K. Xiao\*, **X. Hu**, B. Zhou\* and D.Z. Chen, “Shell: A spatial decomposition data structure for ray traversal on GPU,” *IEEE Transactions on Computers (IEEE TC)*, Vol. 65, No. 1, 2016, pp. 230–243.
65. S. Hong\*, T. Chantem\* and **X. Hu**, “Local-deadline assignment for distributed real-time systems,” *IEEE Transactions on Computers (IEEE TC)*, Vol. 64, No. 7, 2015, pp. 1983–1997.
66. F.A. Shah, G. Csaba, M.T. Niemier, **X. Hu**, W. Porod and G. Bernstein, “Error analysis for ultra dense nanomagnet logic circuits,” *Journal of Applied Physics (JAP)*, Vol. 117, No. 17, 2015, 17A906.
67. C. Leng, Y. Qiao, **X. Hu** and H. Wang, “Utilization-based admission control for aperiodic tasks under EDF scheduling,” *Real-Time Systems*, Vol. 51, No. 1, 2015, pp. 36–76.
68. B. Sedighi\*, **X. Hu**, H. Liu, J.J. Nahas and M.T. Niemier, “Analog circuit design using tunnel-FETs,” *IEEE Transactions on Circuits and Systems I (IEEE TCAS I)*, Vol. 62, No. 1, 2015, pp. 39–48.
69. B. Sedighi\*, **X. Hu**, J.J. Nahas and M.T. Niemier, “Nontraditional computation using beyond-CMOS tunneling devices,” *IEEE Journal of Emerging and Selected Topics in Circuits and Systems (IEEE JETCAS)*, Vol. 4, No. 4, 2014, pp. 438–449.
70. Y. Wang, Y. Liu, S. Li, X. Sheng, D. Zhang, M.-F. Chiang, B. Sai, **X. Hu** and H. Yang, “PaCC: a parallel compare and compress codec for area reduction in nonvolatile processors,” *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 22, No. 7, 2014, pp. 1491–1505.
71. A. Papp, M.T. Niemier, A. Csurgay, M. Becherer, S. Breitzkreutz, J. Kiermaier, I. Eichwald, **X. Hu**, X. Ju, W. Porod and G. Csaba, “Threshold gate based circuits from Nanomagnetic Logic,” *IEEE Transactions on Nanotechnology (IEEE TNANO)*, Vol. 13, No. 5, 2014, pp. 990–996.

72. B. Zhou\*, K. Xiao\*, D.Z. Chen and **X. Hu**, "GPU-optimized volume raytracing for massive numbers of rays," *ACM Transactions on Embedded Computing Systems (ACM TECS)*, Vol. 13, No. 3, December 2013, pp. 42:1–42:17.
73. B. Zhou\*, **X. Hu**, D.Z. Chen and C.X. Yu, "Accelerating radiation dose calculation: a multi-FPGA solution," *ACM Transactions on Embedded Computing Systems (ACM TECS)*, Vol. 13, No. 1s, November 2013, pp. 33:1–33:25.
74. M.A. Siddiq, M.T. Niemier, G. Csaba, A.O. Orlov, **X. Hu**, W. Porod and G.H. Bernstein, "A nanomagnet logic field-coupled electrical input," *IEEE Transaction on Nanotechnology (IEEE TNANO)*, Vol. 12, No. 5, September 2013, pp. 734–742.
75. P. Li, G. Csaba, M.T. Niemier, **X. Hu**, J. Nahas, W. Porod and G.H. Bernstein, "Power reduction in nanomagnet logic clocking through high permeability dielectrics," *Journal of Applied Physics (JAP)*, Vol. 113, No. 17, May, 2013, pp. 17B906–17B906-3.
76. S. Liu\*, **X. Hu**, M.T. Niemier, J.J. Nahas, G. Csaba, G.H. Bernstein and W. Porod, "Exploring the design of the magnetic-electrical interface for nanomagnet logic," *IEEE Transaction on Nanotechnology (IEEE TNANO)*, Vol. 12, No. 2, March 2013, pp. 203–214.
77. K. Xiao\*, D.Z. Chen, **X. Hu** and B. Zhou\*, "Efficient implementation of the 3D-DDA ray traversal algorithm on GPU and its application in radiation dose calculation," *Medical Physics*, Vol 39, No. 12, Dec. 2012, pp. 7619–7625.
78. P. Li, V.K. Sankar, G. Csaba, **X. Hu**, M. Niemier, W. Porod and G.H. Bernstein, "Magnetic properties of enhanced permeability dielectrics for nanomagnetic logic circuits," *IEEE Transactions on Magnetics*, Vol. 48, No. 11, Nov. 2012, pp. 3292–3295.
79. P. Li, G. Csaba, V.K. Sankar, X. Ju, E. Varga, P. Lugli, **X. Hu**, M. Niemier, W. Porod and G.H. Bernstein, "Direct measurement of magnetic coupling between nanomagnets for nanomagnetic logic applications," *IEEE Transactions on Magnetics*, Vol. 48, No. 11, Nov. 2012, pp. 4402–4405.
80. P. Li, G. Csaba, V.K. Sankar, X. Ju, P. Lugli, **X. Hu**, M. Niemier, W. Porod, G.H. Bernstein, "Switching behavior of lithographically fabricated nanomagnets for logic applications," *Journal of Applied Physics (JAP)*, Vol. 111, No. 7, April 2012, pp. 07B911–07B911-3.
81. M.T. Alam, S. Kurtz\*, M.A. Siddiq, M.T. Niemier, G.H. Bernstein, **X. Hu** and W. Porod, "On-chip clocking of nanomagnet logic lines and gates," *IEEE Transaction on Nanotechnology (IEEE TNANO)*, Vol. 11, No. 2, March 2012, pp. 273–286.
82. M. Niemier, E. Varga, G.H. Bernstein, W. Porod, M.T. Alam, A. Dingler\*, A. Orlov and **X. Hu**, "Shape engineering for non-majority boolean gate designs with nanomagnet logic," *IEEE Transactions on Nanotechnology (IEEE TNANO)*, Vol. 11, No. 2, March 2012, pp. 220–230.
83. M. Crocker\*, M. Niemier and **X. Hu**, "A reconfigurable PLA architecture for nanomagnet logic," *ACM Journal on Emerging Technologies in Computing Systems (ACM JETC)*, Vol. 8, No. 1, February 2012, pp. 1:1–1:25.



84. M. T. Niemier, G. H. Bernstein, G. Csaba, A. Dingler\*, **X. Hu**, S. Kurtz, S. Liu, J. Nahas, W. Porod, M.A. Siddiq and E. Varga, "Nanomagnet logic: progress toward system-level integration," *Journal of Physics: Condensed Matter*, Vol. 23, No. 49, December 2011, pp. 493202 (35 pages).
85. T. Chantem\*, **X. Hu** and R.P. Dick, "Temperature-aware scheduling and assignment for hard real-time applications on MPSoCs," *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 19, No. 10, October 2011, pp. 1884–1897.
86. S. Liu\*, **X. Hu**, J.J. Nahas, M. Niemier, W. Porod and G.H. Bernstein, "Magnetic-electrical interface for nanomagnet logic," *IEEE Transactions on Nanotechnology (IEEE TNANO)*, Vol. 10, No. 4, July 2011, pp. 757–763.
87. N. Bansal, D.Z. Chen, D. Coppersmith, **X. Hu**, S. Luan, E. Misiolek, B. Schieber and C. Wang, "Shape rectangularization problems in intensity-modulated radiation therapy," *Algorithmica*, Vol. 60, No. 2, June 2011, pp. 421–450.
88. J. Yi, C. Poellabauer, **X. Hu** and L. Zhang, "Minimum bandwidth reservations for periodic streams in wireless real-time systems," *IEEE Transactions on Mobile Computing (IEEE TMC)*, Vol. 10, No. 4, April 2011, pp. 479–490.
89. S. Kurtz\*, E. Varga, M. Niemier, W. Porod, **X. Hu** and G. H. Bernstein, "Non-majority magnetic logic gates: a review of experiments and future prospects for 'shape-based' logic," invited, *Journal of Physics: Condensed Matter*, Vol. 23, No. 5, February 2011, pp. 053202 (13 pages).
90. A. Dingler\*, M. Niemier, **X. Hu** and E. Lent\*, "Performance and energy impact of locally controlled NML circuits," *ACM Journal on Emerging Technologies in Computing Systems (ACM JETC)*, Vol. 7, No. 1, January 2011, pp. 2:1–2:24.
91. B. Zhou\*, C.Y. Yu, D.Z. Chen and **X. Hu** "GPU-accelerated Monte Carlo convolution/superposition implementation for dose calculation," *Medical Physics*, Vol 37, No. 11, Nov. 2010, pp. 5593–5603.
92. E. Varga, A. Orlov, M. Niemier, **X. Hu**, G.H. Bernstein and W. Porod, "Experimental demonstration of fanout for nanomagnetic logic," *IEEE Transactions on Nanotechnology (IEEE TNANO)*, Vo. 9, No. 6, pp. 668–670, 2010.
93. J. Yi, C. Poellabauer, **X. Hu**, T. Chantem\* and L. Zhang, "Dynamic channel reservations for wireless multihop communications," *Mobile Computing and Communications Review*, Vol. 14, No. 3, July 2010, pp. 43–45.
94. M.T. Alam, M.A. Siddiq, G.H. Bernstein, M. Niemier, W. Porod and **X. Hu**, "On-chip clocking for nanomagnet logic devices," *IEEE Transactions on Nanotechnology (IEEE TNANO)*, Vol. 9, No. 3, May 2010, pp. 348–351.
95. Y. Yu, S. Ren and **X. Hu**, "A metric for quantifying similarity between timing constraint sets in real-time systems," *ACM Transactions on Design Automation of Electronic Systems (ACM TODAES)*, Vol. 9, No. 4, April 2010, pp. 33:1–33:24.

96. M. Crocker\*, **X. Hu** and M. Niemier, "Defects and faults in QCA-Based PLAs", *ACM Journal on Emerging Technologies in Computing Systems (ACM JETC)*, Vol. 5, No. 2, July 2009, pp. 8:1–8:27.
97. G. Quan\*, L. Niu, B. Mochocki\* and **X. Hu**, "Fixed-priority scheduling to reduce both the dynamic and leakage energy on variable voltage processors," *International Journal of Embedded Systems*, a special issue on low-power real-time embedded computing, Vol. 4, No. 2, 2009, pp. 127–140.
98. T. Chantem\*, **X. Hu** and M.D. Lemmon, "Generalized elastic scheduling for real-time tasks," *IEEE Transactions on Computers (IEEE TC)*, Vol. 58, No. 4, April 2009, pp. 480–495.
99. P. Kalla\*, **X. Hu** and J. Henkel, "A flexible framework for communication evaluation in SoC design," the Special Issue of *International Journal of Parallel Programming (IJPP)*, Vol. 36, No. 5, October 2008, pp. 457–477.
100. M. Crocker\*, **X. Hu**, M. Niemier, M. Yan and G. Bernstein, "PLAs in Quantum-dot Cellular Automata," *IEEE Transactions on Nanotechnology (IEEE TNANO)*, Vol. 7, No. 3, May 2008, pp. 376–386.
101. D.Z. Chen, **X. Hu**, S. Luan, C. Wang and X. Wu, "Mountain Reduction, Block Matching, and Applications in Intensity-Modulated Radiation Therapy," an **invited paper** to the Special Issue of *International Journal of Computational Geometry and Applications (IJCGA)* on Selected Papers from the *21st Annual ACM Symp. on Computational Geometry (SCG)*, Vol. 18, No. 1/2, April 2008, pp. 63–106.
102. M. Crocker\*, M.T. Niemier, **X. Hu** and M. Lieberman, "Molecular QCA design with chemically reasonable constraints," *ACM Journal on Emerging Technologies in Computing Systems (ACM JETC)*, Vol. 4, No. 2, April 2008, pp. 9:1–9:21.
103. A. Chaudhary, D.Z. Chen, **X. Hu**, M.T. Niemier, R. Ravichandran and K. Whitton, "Fabricatable Interconnect and Molecular QCA Circuits," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 26, No. 11, November 2007, pp. 1978–1991.
104. G. Quan\* and **X. Hu**, "Energy efficient DVS schedule for fixed-priority real-time systems," *ACM Transactions on Embedded Computing Systems (ACM TECS)*, Vol. 6, No. 4, September 2007, pp. 29:1–29:31.
105. B. Mochocki\*, **X. Hu** and G. Quan\*, "Transition overhead aware voltage scheduling for fixed-priority real-time systems," *ACM Transactions on Design Automation of Electronic Systems (ACM TODAES)*, Vol. 12, No. 2, April 2007, pp. 11:1–11:26.
106. G. Quan\*, G. Greenwood, D. Liu\* and **X. Hu**, "Searching for multiobjective preventive maintenance schedules: Combining preferences with evolutionary algorithms," *European Journal of Operational Research*, Vol. 177, No. 3, March 2007, pp. 1969–1984.
107. D.Z. Chen, **X. Hu**, S. Luan, C. Wang, S.A. Naqvi, and C.X. Yu, "Generalized geometric approaches for leaf sequencing problems in radiation therapy," An **invited paper** to

- the Special Issue of *International Journal of Computational Geometry and Applications (IJCGA)* on Selected Papers from the *15th Annual International Symposium on Algorithms and Computation (ISAAC)*, Hong Kong, December 2004, Vol. 16, No 2-3, June 2006, pp. 175–204.
108. S. Luan, C. Wang, D.Z. Chen, **X. Hu**, S.A. Naqvi, X. Wu, and C.X. Yu, “An improved MLC segmentation algorithm and software for step-and-shoot IMRT delivery without tongue-and-groove error,” *Medical Physics*, Vol. 33, Issue 5, May 2006, pp. 1199–1212.
  109. D. Liu\*, **X. Hu**, M. Lemmon and Q. Ling, “Firm real-time system scheduling based on a novel QoS constraint,” *IEEE Transactions on Computers (IEEE TC)*, Vol. 55, No. 3, March 2006, pp. 320–333.
  110. P. Kalla\*, **X. Hu** and J. Henkel, “DRU: An enhancement to instruction cache replacement policies for transition energy reduction,” *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 14, No. 1, January 2006, pp. 69-80.
  111. D.Z. Chen, **X. Hu**, S. Luan, X. Wu, and C.X. Yu, “Optimal terrain construction problems and applications in intensity-modulated radiation therapy,” an **invited paper** in the Special Issue of *Algorithmica* on Selected Papers from the *Tenth Annual European Symposium on Algorithms* (2002), Vol. 42, No. 3-4, June 2005, pp. 265–288.
  112. Z. Wang\* and **X. Hu**, “Energy-aware variable partitioning and instruction scheduling for multibank memory architectures,” *ACM Transactions on Design Automation of Electronic Systems (ACM TODAES)*, Vol. 10, No. 2, 2005, pp. 369–388.
  113. D.Z. Chen, **X. Hu**, S. Luan, C. Wang and X. Wu, “Geometric algorithms for static leaf sequencing problems in radiation therapy,” an **invited paper** in the Special Issue of the *International Journal of Computational Geometry and Applications (IJCGA)* on Selected Papers from the *19th Annual ACM Symposium on Computational Geometry* (2003), Vol. 14, No. 5, 2005, pp. 311–339.
  114. B. Mochocki\*, **X. Hu** and G. Quan\*, “A unified approach to variable voltage scheduling for non-ideal DVS processors,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 23, No. 9, 2004, pp. 1370–1377.
  115. S. Luan, C. Wang, D.Z. Chen, **X. Hu**, S. A. Naqvi, C.X. Yu and C.L. Lee, “A new MLC segmentation algorithm/software for step-and-shoot IMRT delivery,” *Medical Physics*, Vol. 31, No. 4, 2004, pp. 695–707.
  116. G. Quan\* and **X. Hu**, “Minimal energy fixed-priority scheduling for variable voltage processors,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 22, No. 8, 2003, pp. 1062–1071.
  117. D.Z. Chen, **X. Hu** and J. Xu, “Computing optimal beams in two and three dimensions,” *Journal of Combinatorial Optimization*, Vol. 7, No. 2, 2003, pp. 111–136.
  118. D.Z. Chen, **X. Hu**, O. Daescu and J. Xu, “Finding an optimal path without growing the tree,” an invited paper in the Special Issue of *Journal of Algorithms* on Selected Papers from the *Sixth Annual European Symposium on Algorithms* (1998), Vol. 49, No. 1, 2003, pp. 13–41.

119. H. Liu\* and **X. Hu**, “Processor utilization bounds for real-time systems with precedence constraints,” *Journal of Design Automation for Embedded Systems*, Special Issue on Design Methodologies and Tools for Real-Time Embedded Systems, Vol. 7, No. 1-2, 2002, pp. 89–113.
120. Y. Zhang\*, **X. Hu** and D.Z. Chen, “Efficient global register allocation for minimizing energy consumption,” *ACM SIGPLAN Notices*, Vol. 37, No. 4, 2002, pp. 42–53. (SIGPLAN stands for the ACM Special Interest Group on Programming Languages.)
121. D.Z. Chen, **X. Hu** and X. Wu, “Optimal polygon cover problems and applications,” an **invited paper** in the Special Issue of the *International Journal of Computational Geometry and Applications (IJCGA)* on Selected Papers from the *Eleventh Annual International Symposium on Algorithms and Computation (ISAAC)* (2000), Vol. 12, No. 4, 2002, pp. 309–338.
122. Y. Zhang\*, **X. Hu** and D.Z. Chen, “Cell selection from technology libraries for minimizing power,” *Integration, the VLSI Journal*, Vol. 31, No. 2, 2002, pp. 133–158.
123. T. Zhou\*, **X. Hu** and E.H.-M. Sha, “Estimating probabilistic timing performance for real-time embedded systems,” *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 9, No. 6, 2001, pp. 833–844.
124. D.Z. Chen, O. Daescu, **X. Hu**, X. Wu and J. Xu, “Determining an optimal penetration among weighted regions in two and three dimensions,” *Journal of Combinatorial Optimization* for a Special Issue on Optimization Problems in Medical Applications, Vol. 5, No. 1, 2001, pp. 59–79.
125. **X. Hu**, D.Z. Chen and R. Sambandam\*, “Efficient list-approximation techniques for floor-plan area minimization,” *ACM Transactions on Design Automation of Electronic Systems (ACM TODAES)*, Vol. 6, No. 3, 2001, pp. 372–400.
126. R. Sambandam\* and **X. Hu**, “Multi-valued performance metrics for real-time embedded systems,” with R. Sambandam, *Journal of Design Automation for Embedded Systems*, Vol. 5, No. 1, 2000, pp. 5–28.
127. C. Chantrapornchai, E.H.-M. Sha and **X. Hu**, “Efficient module selections for finding highly acceptable designs based on inclusion scheduling,” *Journal of System Architectures (JSA)*, Vol. 46, No. 11, 2000, pp. 1047–1071.
128. C. Chantrapornchai, E.H.-M. Sha and **X. Hu**, “Efficient acceptable design exploration based on module utility selection,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 19, No. 1, 2000, pp. 19–29.
129. G.W. Greenwood and **X. Hu**, “On the use of random walks to estimate correlation in fitness landscapes,” *Journal of Computational Statistics and Data Analysis*, Vol. 28, No. 2, January 1998, pp. 131–137.
130. **X. Hu** and G.W. Greenwood, “An evolutionary approach to hardware/software partitioning,” *IEE Proceedings—Computers and Digital Techniques, Special Issue on Hardware/Software Codesign for Embedded Systems*, Vol. 145, No. 3, May 1998, pp. 203–209.

131. G.W. Greenwood and **X. Hu**, “Are landscapes for constrained optimization problems statistically isotropic?” *Physica Scripta*, Vol. 57, 1998, pp. 321–323.
132. **X. Hu** and J.G. D’Ambrosio, “Hardware/software partitioning for real-time embedded systems,” *Journal of Design Automation for Embedded Systems*, Vol. 2, No. 3/4, May 1997, pp. 339–358.
133. D.Z. Chen and **X. Hu**, “Fast and efficient operations on parallel priority queues,” *Parallel Processing Letters*, Vol. 6, No. 4, December 1996, pp. 451–467.
134. **X. Hu**, S.C. Bass and R.G. Harber, “Minimizing the number of delay buffers in the synchronization of pipelined systems,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 13, No. 12, December 1994, pp. 1441–1449.
135. J.G. D’Ambrosio, **X. Hu**, B.T. Murray and D. Tang, “Codesign of architectures for automotive powertrain modules,” *IEEE Micro*, August 1994, pp. 17–25.
136. **X. Hu**, S.C. Bass and R.G. Harber, “An efficient implementation of singular value decomposition rotation transformation with CORDIC processors,” *Journal of Parallel and Distributed Computing (JPDC)*, Vol. 17, April 1993, pp. 360–362.
137. **X. Hu**, R.G. Harber and S.C. Bass, “Expanding the range of convergence of the CORDIC algorithm,” with R.G. Harber and S.C. Bass, *IEEE Transactions on Computers (IEEE TC)*, Vol. 40, No. 1, January 1991, pp. 13–21.

## Refereed Conference Papers (published or accepted for publication)

1. M. Chang, X. Yin\*, Z. Toroczkai, **X. Hu** and A. Raychowdhury, “An analog clock-free compute fabric based on continuous-time dynamical system for solving combinatorial optimization problems,” accepted to *IEEE Custom Integrated Circuits Conference (CICC)* (IEEE), April 2022.
2. Z. Yan\*, W. Jiang, **X. Hu** and Y. Shi, “RADARS: Memory efficient reinforcement learning aided differentiable neural architecture search,” accepted to *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2022.
3. R. Rajaei\*, M. Niemier and **X. Hu**, “Low-cost sequential logic circuit design considering single event double-node upsets and single event transients,” *IEEE International Conference on Computer Design (ICCD)*, (IEEE), September 2021, pp. 178–185.
4. A. Kazemi\*, S. Sahay, A. Saxena, M. M. Sharifi\*, M. Niemier and **X. Hu**, “A flash-based multi-bit content-addressable memory with Euclidean squared distance,” *International Symposium on Low Power Electronics and Design (ISLPED)* (IEEE/ACM), July 2021, 6 pages.
5. A. Kazemi\*, M. M. Sharifi\*, Z. Zou, M. Niemier, **X. Hu** and M. Imani, “MIMHD: Accurate and efficient hyperdimensional inference using multi-bit In-memory computing,” *International Symposium on Low Power Electronics and Design (ISLPED)* (IEEE/ACM), July 2021, 6 pages.
6. M. M. Sharifi\*, L. Pentecost, R. Rajaei\*, A. Kazemi\*, Q. Lou\*, G-Y. Wei, D. Brooks, K. Ni, **X. Hu**, M. Niemier and M. Donato, “Application-driven design exploration for dense ferroelectric embedded non-volatile memories,” *International Symposium on Low Power Electronics and Design (ISLPED)* (IEEE/ACM), July 2021, 6 pages.
7. M. Yang, M. R. Jokar, J. Qiu, Q. Lou\*, Y. Liu, A. Udupa, F. T. Chong, J. M. Dallesasse, M. Feng, L. L. Goddard, **X. Hu** and Y. Li, “A hybrid optical-electrical analog deep learning accelerator using incoherent optical signals,” *Great Lakes Symposium on VLSI (GLSVLSI)* (ACM), June 2021, pp. 271–276.
8. J. Wang, T. Zhang\*, D. Shen\*, **X. Hu** and S. Han, “APaS: An adaptive partition-based scheduling framework for 6TiSCH networks,” *IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)* (IEEE), May 2021, pp. 320–332.
9. S. Thomann, C. Li, C. Zhuo, O. Prakash, X. Yin\*, **X. Hu** and H. Amrouch, “On the reliability of in-memory computing: impact of temperature on ferroelectric TCAM,” *IEEE VLSI Test Symposium (VTS)* (IEEE), April 2021, pp. 1–6. (Nominated for the **Best Paper Award**.)
10. S. Mishra\*, D. Chen and **X. Hu**, “Objective-dependent uncertainty driven retinal vessel segmentation,” *IEEE International Symposium on Biomedical Imaging (ISBI)* (IEEE), April 2021, pp. 453–457.
11. M. Li\* and **X. Hu**, “A quantization framework for neural network adaption at the edge,” *Design Automation and Test in Europe (DATE)* (ACM/IEEE), 2021, pp. 402–407/

12. A. Kazemi\*, M.M. Sharifi\*, A.F. Laguna\*, F. Mueller, R. Rajaei\*, R. Olivo, T. Kaempfe, M. Niemier and **X. Hu**, “In-memory nearest neighbors with FeFET multi-bit content-addressable memories,” *Design Automation and Test in Europe (DATE)* (ACM/IEEE), 2021, pp. 1084–1089. (Nominated for the **Best Paper** Award.)
13. A.F. Laguna\*, A. Kazemi\*, M. Niemier and **X. Hu**, “In-memory computing based accelerator for transformer networks for long sequences,” *Design Automation and Test in Europe (DATE)* (ACM/IEEE), 2021, pp. 1839–1844.
14. D. Reis\*, A.F. Laguna\*, M. Niemier and **X. Hu**, “Attention-in-memory for few-shot learning with configurable ferroelectric FET arrays,” *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2021, pp. 49–54.
15. J. S. Takeshita, D. Reis\*, T. Gong, M. Niemier, **X. Hu** and T. Jung, “Algorithmic acceleration of B/FV-like somewhat homomorphic encryption for compute-enabled RAM,” *Selected Areas in Cryptography*, 2020.
16. A.F. Laguna\*, H. Gamaarachchi, X. Yin\*, M. Niemier, S. Parameswaran and **X. Hu**, “Seed-and-vote based in-memory accelerator for DNA read mapping,” *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2020. Article No. 56, pp. 1–9.
17. X. Dai, S. Zhao, Y. Jiang, X. Jiao, **X. Hu** and W. Chang, “Fixed-priority scheduling and controller co-design for time-sensitive networks,” *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2020. Article No. 99, pp. 1–9.
18. A. Kazemi\*, R. Rajaei\*, K. Ni, S. Datta, M. Niemier and **X. Hu**, “A hybrid FeMFET-CMOS analog synapse circuit for neural network training and inference,” *International Symposium on Circuits and Systems (ISCAS)* (IEEE), October 2020, pp. 1–5.
19. R. Rajaei\*, Y.-K. Lin, S. Salahuddin, M. Niemier and **X. Hu**, “Dynamic memory and sequential logic design using negative capacitance FinFETs,” *International Symposium on Circuits and Systems (ISCAS)* (IEEE), October 2020, pp. 1–5.
20. R. Rajaei\*, Y.K. Lin, S. Salahuddin, M. Niemier and **X. Hu**, “GC-eDRAM design using hybrid FinFET/NC-FinFET,” *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)* (ACM/IEEE), August 2020, pp. 199–204.
21. Q. Lou\*, T. Gao, P. Faley, M. Niemier, **X. Hu** and S. Joshi, “Embedding error correction into crossbars for reliable matrix vector multiplication using emerging devices,” *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)* (ACM/IEEE), August 2020, pp. 139–144.
22. A. Kazemi\*, C. Alessandri, A. C. Seabaugh, **X. Hu**, M. Niemier and S. Joshi, “A device non-ideality resilient approach for mapping neural networks to crossbar arrays,” *ACM/IEEE Design Automation Conference (DAC)* (ACM/IEEE), July 2020, pp. 1–6.
23. S. Mishra\*, D. Chen and **X. Hu**, “A data-aware deep supervised method for retinal vessel segmentation,” *IEEE International Symposium on Biomedical Imaging (ISBI)* (IEEE), April 2020, pp. 1254–1257.

24. K. Ni, A. Gupta, O. Prakash, S. Thomann, **X. Hu** and H. Amrouch, "Impact of extrinsic variation sources on the device-to-device variation in Ferroelectric FET," *IEEE International Reliability Physics Symposium (IRPS)* (IEEE), March 2020 (5 pages).
25. A. Gupta, K. Ni, O. Prakash, **X. Hu** and H. Amrouch, "Temperature dependence and temperature-aware sensing in Ferroelectric FET," *IEEE International Reliability Physics Symposium (IRPS)* (IEEE), March 2020 (5 pages).
26. D. Reis\*, A.F. Laguna\*, M. Niemier and **X. Hu**, "A fast and energy efficient Computing-in-Memory architecture for few-shot learning applications," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2020, pp. 127–132.
27. M.M. Sharifi\*, R. Rajaei\*, P. Cadareanu, P.-E. Gaillardon, Y. Jin, M. Niemier and **X. Hu**, "A novel TIGFET-based DFF design for improved resilience to power side-channel attacks," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2020, pp. 1253–1258.
28. M. Li\*, X. Yin\*, **X. Hu** and C. Zhuo, "Nonvolatile and energy-efficient FeFET-based multiplier for energy-harvesting devices," *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2020, pp. 562–567.
29. Y. Lin, Q. Zhang, J. Tang, B. Gao, C. Li, P. Yao, Z. Liu, J. Zhu, J. Lu, **X. Hu**, H. Qian and H. Wu, "Bayesian neural network realization by exploiting inherent stochastic behavior of analog RRAM," *IEEE International Electron Devices Meeting (IEDM)* (IEEE), 2019, pp. 14.6.1–14.6.4.
30. I. Palit\*, Q. Lou\*, R. Perricone\*, M. Niemier and **X. Hu**, "A uniform modeling methodology for benchmarking DNN accelerators," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2019 (6 pages).
31. T. Gong, T. Zhang\*, **X. Hu**, Q. Deng, M. Lemmon and S. Han, "Reliable dynamic packet scheduling over lossy real-time wireless network," *Euromicro Conference on Real-Time Systems (ECRTS)*, July 2019, pp. 11:1–11:23.
32. S. Mishra\*, P. Liang, A. Czajka, D. Chen and **X. Hu**, "CC-Net: Image complexity guided network compression for biomedical image segmentation," *IEEE International Symposium on Biomedical Imaging (ISBI)* (IEEE), April 2019, pp. 57–60.
33. L. Li, T. Wei, J. Zhou\*, M. Chen and **X. Hu**, "CE-based optimization for real-time system availability under learned soft error rate," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2019, pp. 1331–1336.
34. A. F. Laguna\*, M. Niemier and **X. Hu**, "Design of hardware-friendly memory enhanced neural networks," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2019, pp. 1583–1586.
35. R. Perricone\*, Z. Liang, M. G. Mankalale, M. Niemier, S. S. Sapatnekar, J.-P. Wang and **X. Hu**, "An energy efficient non-volatile flip-flop based on CoMET technology," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2019, pp. 390–395.



36. D. Zhang, Y. Ma\*, C. Zheng, Y. Zhang, **X. Hu** and D. Wang, “Cooperative-competitive task allocation in edge computing for delay-sensitive social sensing,” *ACM/IEEE Symposium on Edge Computing (SEC)* (ACM/IEEE), October 2018, pp. 243–259.
37. D. Reis\*, M. Niemier and **X. Hu**, “Computing in-memory with FeFETs,” *International Symposium on Low Power Electronics and Design (ISLPED)* (ACM/IEEE), July 2018. Article No. 24, pp. 1–6. (Received the **Best Paper** Award.)
38. X. Xu, Q. Lu, L. Yang, **X. Hu**, D.Z. Chen, Yu. Hu and Y. Shi, “Quantization of fully convolutional networks for accurate biomedical image segmentation,” *IEEE/CVF Conference on Computer Vision and Pattern Recognition (CVPR)* (IEEE), June 2018, pp. 8300–8308.
39. I. Palit\*, L. Yang, Y. Ma\*, D.Z. Chen, M. Niemier, J. Xiong and **X. Hu**, “Biomedical image segmentation using fully convolutional networks on TrueNorth,” to *International Symposium on Computer-Based Medical Systems (CBMS)*, June 2018, pp. 375–380.
40. X. Chen\*, Niemier and **X. Hu**, “Nonvolatile Lookup Table Design Based on Ferroelectric Field-Effect Transistors,” *International Symposium on Circuits and Systems (ISCAS)* (IEEE), May 2018, pp. 1–5.
41. T. Zhang\*, T. Gong, Z. Yun, S. Han, Q. Deng and **X. Hu**, “FD-PaS: A fully distributed packet scheduling framework for handling disturbances in real-time wireless networks,” *IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)* (IEEE), April 2018, pp. 1–12.
42. D. Zhang, Y. Ma\*, Y. Zhang, S. Lin, **X. Hu**, D. Wang, “A real-time and non-cooperative task allocation framework for social sensing applications in edge computing systems,” *IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)* (IEEE), April 2018, pp. 316–326.
43. X. Chen\*, X. Yin\*, M. Niemier and **X. Hu**, “Design and optimization of FeFET-based crossbars for binary convolution neural networks,” *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2018, pp. 1211–1216.
44. X. Chen\*, D.Z. Chen and **X. Hu**, “moDNN: Memory optimal DNN training on GPUs,” *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2018, pp. 13–18.
45. Y. Ma\*, T. Chantem\*, R. P. Dick, and **X. Hu**, “Improving reliability for real-time systems through dynamic recovery,” *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2018, pp. 521–526.
46. W. Chang, D. Roy, **X. Hu** and S. Chakraborty, “Cache-aware task scheduling for maximizing control performance,” *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2018, pp. 700–705.
47. L. Li, P. Cong, K. Cao, J. Zhou\*, T. Wei, M. Chen and **X. Hu**, “Feedback control of real-time EtherCAT networks for reliability enhancement in CPS,” *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2018, pp. 694–699.
48. J. Zhou\*, T. Wei, M. Chen, **X. Hu**, Y. Ma\*, G. Zhang and J. Yan, “Variation-aware task allocation and scheduling for improving reliability of real-time MPSoCs,” *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2018, pp. 171–176.

49. X. Chen\*, J. Chen, D.Z. Chen and **X. Hu**, “Optimizing memory efficiency for convolution kernels on Kepler GPUs,” *Design Automation Conference (DAC)* (ACM/IEEE), June 2017, Article No. 68, 6 pages.
50. Y. Bai, **X. Hu**, R. F. DeMara and M. Lin, “A spin-orbit torque based Cellular Neural Network (CNN) architecture,” *Great Lakes Symposium on VLSI (GLSVLSI)* (ACM), May 2017, pp. 59–64.
51. T. Zhang\*, T. Gong, C. Gu, H. Ji, S. Han, Q. Deng and **X. Hu**, “Distributed dynamic packet scheduling for handling disturbances in real-time wireless networks,” *IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)* (IEEE), April 2017, pp. 261–272.
52. J. Zhou\*, J. Yan, T. Wei, M.Chen and **X. Hu**, “Energy-adaptive scheduling of imprecise computation tasks for QoS optimization in real-time MPSoC systems,” *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2017, pp. 1402–1407.
53. Y. Ma\*, T. Chantem\*, R. Dick and **X. Hu**, “An on-line framework for improving reliability of real-time systems on ‘Big-Little’ type MPSoCs,” *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2017, pp. 446–451.
54. X. Yin\*, M. Niemier and **X. Hu**, “Design and benchmarking of ferroelectric FET based TCAM,” *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2017, pp. 1444–1449.
55. X. Yin\*, A. Aziz, J. Nahas, S. Datta, S. Gupta, M.Niemier and **X. Hu**, “Exploiting ferroelectric FETs for low-power non-volatile logic-in-memory circuits,” *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2016, pp. 121–126.
56. C. Gu\*, N. Guan, Z.Feng, Q. Deng, **X. Hu** and Y. Wang, “ Transforming real-time task graphs to improve schedulability,” *IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA)* (IEEE), August 2016, pp. 29–38. (Nominated for the **Best Paper** Award.)
57. X. Yin\*, B. Sedighi\*, M. Niemier and **X. Hu**, “Design of latches and flip-flops using emerging tunneling devices,” *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2016, pp. 367–372.
58. T. Liu, H. Guo, S. Parameswaran and **X. Hu**, “Improving tag generation for memory data authentication in embedded processor systems,” *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2016, pp. 50–55.
59. J. Zhou\*, **X. Hu**, Y. Ma\* and T. Wei, “Balancing lifetime and soft-error reliability to improve system availability,” *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2016, pp. 685–690.
60. A. Tan, Q. Wang, N. Guan, Q. Deng and **X. Hu**, “Inter-cell channel time-slot scheduling for multichannel multiradio cellular fieldbuses,” *IEEE real-time symposium (RTSS)* (IEEE), December 2015, pp. 227–238.

61. I. Palit\*, Q. Lou, N. Acampora, J. Nahas, M.T. Niemier, **X. Hu**, “Analytically modeling power and performance of a CNN system,” *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2015, pp. 186–193.
62. K. Shamsi, Y. Bi, Y. Jin, P.-E. Gaillardon, M. Niemier and **X. Hu**. “Reliable and high performance STT-MRAM architectures based on controllable-polarity devices,” *IEEE International Conference on Computer Design (ICCD)*, (IEEE), pp. 372–379, October 2015.
63. S. Arunachalam, T. Chantem\*, R.P. Dick and **X. Hu**, “An online wear state monitoring methodology for off-the-shelf embedded processors,” *International Conference on Hardware/Software Co-Design and System Synthesis (CODES+ISSS)* (IEEE), October 2015, pp. 114–123.
64. S. Hong\*, **X. Hu**, T. Gong and S. Han, “On-line data link layer scheduling in wireless networked control systems,” *Euromicro Conference on Real-Time Systems (ECRTS)*, pp. 57–66. July 2015.
65. K. Xiao\*, D.Z. Chen, **X. Hu** and B. Zhou\*, “Monte Carlo based ray tracing in CPU-GPU heterogeneous systems and applications in radiation therapy,” *ACM Symposium on High-Performance Parallel and Distributed Computing (HPDC)*, (ACM), pp. 247–258, June 2015.
66. Y. Ma\*, T. Chantem\*, **X. Hu** and Robert P. Dick: “Improving lifetime of multicore soft real-time systems through global utilization control,” *ACM Great Lakes Symposium on VLSI (GLVLSI)* (ACM), May 2015, pp. 79–82.
67. Q. Lou\*, I. Palit\*, A. Horvath, **X. Hu**, M. T. Niemier, J. Nahas, “TFET-based operational transconductance amplifier design for CNN systems,” *ACM Great Lakes Symposium on VLSI (GLVLSI)* (ACM), May 2015, pp. 277–282.
68. A. Kiss, Z. Nagy, P. Szolgay, G. Csaba, **X. Hu** and W. Porod, “Emulating massively parallel non-Boolean operators on FPGA,” *International Symposium on Circuits and Systems (ISCAS)* (IEEE), May 2015, pp. 1981–1984.
69. L. Tang\*, **X. Hu**, R. Barrett, “PerDome: a performance model for heterogeneous computing systems,” *High Performance Computing Symposium (HPC)*, (ACM), April 2015, pp. 225–232.
70. B. Sedighi\*, I. Palit\*, **X. Hu**, J. Nahas and Michael Niemier, “A CNN-inspired mixed signal processor based on tunnel transistors,” *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2015, pp. 1150–1155.
71. R. Perricone\*, Y. Zhu\*, K.M. Sanders\*, **X. Hu** and M. Niemier, “Towards systematic design of 3D pNML layouts,” *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2015, pp. 1539–1542.
72. Y. Bi, P.E. Gaillardon, **X. Hu**, M.T. Niemier, J. Yuan and Y. Jin, “Leveraging emerging technology for hardware security - case study on silicon nanowire FETs and graphene SymFETs,” *IEEE Asian Test Symposium (ATS)* (IEEE), November 2014, pp. 342–347.

73. F.A. Shah, G. Csaba, M.T. Niemier, **X. Hu**, W. Porod and G.H. Bernstein, "Error analysis for ultra dense nanomagnet logic circuits," *Annual Magnetism and Magnetic Materials Conference (MMM)* (IEEE), November 2014.
74. B. Sedighi\*, J.J. Nahas, M.T. Niemier and **X. Hu**, "Boolean circuit design using emerging tunneling devices," *International Conference on Computer Design (ICCD)* (IEEE), October 2014, pp 355–360.
75. D. Zhang, S. Li, A. Li, Y. Liu, **X. Hu** and H. Yang, "Intra-task scheduling for storage-less and converter-less solar-powered nonvolatile sensor nodes," *International Conference on Computer Design (ICCD)* (IEEE), October 2014, pp 348–354.
76. K. Xiao\*, B. Zhou\*, D.Z. Chen and **X. Hu**, "Efficient Monte Carlo dose calculation on CPU-GPU heterogeneous systems," *Fifty-sixth Annual Meeting and Technical Exhibition of the American Association of Physicists in Medicine (AAPM), Medical Physics*, Vol. 41, No. 6, July 2014.
77. B. Zhou\*, **X. Hu** and D.Z. Chen, "Light Emitting Memory: a modular LED panel with 10K true color frame rate for 3D display applications," *Society for Information Display (SID) Symposium Digest of Technical Papers*, June 2014, pp. 918–921.
78. R. Perricone\*, **X. Hu**, J.J. Nahas and M.T. Niemier, "Design of 3D nanomagnetic logic circuits: a full-adder case study," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2014, pp. 1–6.
79. P. Li, F. Shah, G. Csaba, M.T. Niemier, **X. Hu**, J. Nahas, W. Porod and G.H. Bernstein, "Application of "snow jet" process in fabrication of nanomagnet logic devices," *Annual Magnetism and Magnetic Materials Conference (MMM)* (IEEE), November 2013.
80. P. Li, F. Shah, G. Csaba, M.T. Niemier, **X. Hu**, J. Nahas, W. Porod and G.H. Bernstein, "Power reduction in nanomagnet logic using high-permeability dielectrics," *SRC TECHCON*, September 2013.
81. D.Z. Chen, **X. Hu**, K. Xiao\* and B. Zhou\*, "Shell: a spatial decomposition data structure for 3D curve traversal on many-core architectures," *European Symposium on Algorithms (ESA)*, September 2013, pp. 815–826.
82. A. Kiss, Z. Nagy, P. Szogay, T. Roska, G. Csaba, **X. Hu** and W. Porod, "FPGA-implementation of a holographic pattern-matching algorithm," *European Conference on Circuit Theory and Design (ECCTD)*, September 2013, pp. 1–4.
83. K. Xiao\*, B. Zhou\*, **X. Hu**, D.Z. Chen, "Accelerating collapsed cone convolution/superposition dose calculation on GPU using spatial decomposition," *Fifty-Fifth Annual Meeting and Technical Exhibition of the American Association of Physicists in Medicine (AAPM), Medical Physics*, Vol. 40, No. 6, August 2013.
84. M. Song, S. Li, S. Ren, S. Hong and **X. Hu**, "Computation efficiency driven job removal policies for meeting end-to-end deadlines in distributed real-time systems," *International Symposium on Object/Component/Service-Oriented Real-Time Distributed Computing (ISORC)* (IEEE), June 2013, pp 1–8.

85. S. Liu\*, G. Csaba, **X. Hu**, E. Varga, M.T. Niemier, G. Bernstein and W. Porod, “Minimum-energy state guided physical design for nanomagnet logic,” *Design Automation Conference (DAC)* (ACM/IEEE), June 2013. Article No. 106, pp. 1–7.
86. F.A. Shah, G. Csaba, M.T. Niemier, **X. Hu**, W. Porod and G.H. Bernstein, “Sub-10-nm inter-magnet spacing for improved defect tolerance in NML,” *Electronic Material Conference (EMC)*, June 2013.
87. V.K. Sankar, P. Li, S. Liu\*, F. Shah, H. Dey, G. Csaba, M. Niemier, **X. Hu**, J. Nahas, W. Porod and G.H. Bernstein, “Pseudo-Spin-Valve giant magnetoresistance structures for electronic readout in nanomagnet logic,” *Electronic Material Conference (EMC)*, June 2013.
88. P. Li, F. Shah, G. Csaba, M. Niemier, **X. Hu**, J. Nahas, W. Porod and G.H. Bernstein, “Magnetic properties and thermal stability of nanomagnets/high-permeability dielectrics system,” *Electronic Material Conference (EMC)*, June 2013.
89. Li Tang\*, **X. Hu**, D.Z. Chen, M.T. Niemier, R.F. Barrett, S.D. Hammond and M.-Y. Hsieh, “GPU Acceleration of data assembly in finite element methods and its energy implications,” *IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)* (IEEE), June 2013, pp. 321–328.
90. P. Li, G. Csaba, M. Niemier, **X. Hu**, J. Nahas, W. Porod and G.H. Bernstein, “Vibrating sample magnetometry study of high-permeability dielectrics on nanomagnets,” *International Conference on Frontiers of Characterization and Metrology for Nanoelectronics (FCMN)*, March 2013, (full paper).
91. T. Chantem\*, Y. Xiang, **X. Hu** and R.P. Dick, “Enhancing multicore reliability through wear compensation in online assignment and scheduling,” *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2013, pp. 1373–1378.
92. I. Palit\*, **X. Hu**, J. Nahas and M. Niemier, “Systematic design of nanomagnet logic circuits,” *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2013, pp. 1795–1800.
93. X. He, S. Li, Y. Liu, **X. Hu** and H. Yang, “Utilizing voltage-frequency islands in C-to-RTL synthesis for streaming applications,” *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2013, pp. 992–995.
94. S. Li, Y. Liu, **X. Hu**, X. He, Y. Zhang, P. Zhang and H. Yang, “Optimal partition with block-level parallelization in C-to-RTL synthesis for streaming applications,” *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2013, pp. 225–230. (Nominated for the **Best Paper Award**.)
95. M. Hong, H. Guo and **X. Hu**, “A cost-effective tag design for memory data authentication in embedded systems,” *International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)*, (ACM/IEEE), October 2012. pp. 17–26. (Nominated for the **Best Paper Award**.)

96. S. Kurtz\*, A. Dingler\*, M.T. Niemier, **X. Hu**, G. Csaba, J. Nahas, W. Porod and G.H. Bernstein, "Preserving steady state non-volatility in nanomagnet logic circuits," *SRC TECHCON: Technology and Talent for the 21st Century*, September 2012.
97. P. Li, G. Csaba, V. Sankar, X. Ju, E. Varga, P. Lugli, **X. Hu**, M.T. Niemier, W. Porod and G.H. Bernstein, "Direct measurement of magnetic coupling between nanomagnets for nanomagnet logic applications," *SRC TECHCON: Technology and Talent for the 21st Century*, September 2012.
98. M. Siddiq, G.H. Bernstein, M.T. Niemier, W. Porod and **X. Hu**, "Experimental demonstration of field-coupled input scheme for nanomagnet logic (NML)," *SRC TECHCON: Technology and Talent for the 21st Century*, September 2012.
99. M.T. Niemier, X. Ju, M. Becherer, G. Csaba, A. Dingler\*, **X. Hu**, D. Schmitt-Landsiedel, P. Lugli and W. Porod, "Boolean and non-Boolean architectures for out-of-plane nanomagnet logic," *International Workshop on Cellular Nanoscale Networks and their Applications*, August 2012.
100. M. Niemier, X. Ju, M. Becherer, G. Csaba, **X. Hu**, D. Schmitt-Landsiedel, P. Lugli and W. Porod, "Systolic architectures and applications for nanomagnet logic," *Silicon Nanoelectronics Workshop*, June 2012.
101. A. Dingler\*, S. Kurtz\*, M.T. Niemier, **X. Hu**, G. Csaba, J. Nahas, W. Porod, G. Bernstein, P. Li and V.K. Sankar, "Making non-volatile nanomagnet logic non-volatile," *Design Automation Conference (DAC) (ACM/IEEE)*, June 2012, pp. 476–485.
102. P. Li, G. Csaba, V. K. Sankar, X. Ju, **X. Hu**, M. Niemier, W. Porod and G. H. Bernstein, "Direct measurement of magnetic coupling between nanomagnets for NML applications," *Intermag conference*, May 2012. (Accepted for oral presentation, and nominated for the Best Student Presentation Award.)
103. P. Li, V. K. Sankar, G. Csaba, F. Shah, **X. Hu**, M. Niemier, W. Porod and G. H. Bernstein, "Enhanced permeability dielectrics for power reduction in NML circuits," *Intermag conference*, May 2012. (Accepted for oral presentation.)
104. **X. Hu**, S. Hong\* and M. Lemmon, "Supporting coordinated negotiation in CPS Design," *ACM/IEEE International Conference on Cyber-Physical Systems (ICCPs) (ACM/IEEE)*, Work-In-Progress Session, April 2012.
105. S. Hong\*, T. Chantem\* and **X. Hu**, "Meeting end-to-end deadlines through distributed local deadline assignment," *IEEE real-time symposium (RTSS) (IEEE)*, pp. 183–192, December 2011.
106. P. Li, G. Csaba, V. K. Sankar, **X. Hu**, M. Niemier, W. Porod and G.H. Bernstein, "Switching behavior of lithographically fabricated nanomagnets for logic applications," *Annual Conference on Magnetism & Magnetic Materials (MMM) (IEEE)*, October 2011.
107. S. Liu\*, **X. Hu**, M.T. Niemier, J. Nahas, G. H. Bernstein and W. Porod, "Exploring the design of magnetic-electrical interface for nanomagnet logic," *TECHCON*, September 2011.

108. T. Chantem\*, J. Yi, S. Hong\*, **X. Hu**, C. Poellabauer and L. Zhang, “An online holistic scheduling framework for energy-constrained wireless real-time systems,” *IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA)* (IEEE), August 2011, pp. 267–276.
109. B. Zhou\*, C.Y. Yu, K. Xiao\*, **X. Hu** and D.Z. Chen, “Treatment plan validation through graphical fingerprint,” *Fifty-Third Annual Meeting and Technical Exhibition of the American Association of Physicists in Medicine (AAPM)*, August 2011. *Medical Physics*, Vol. 38, No. 6, 2011.
110. B. Zhou\*, C.Y. Yu, K. Xiao\*, **X. Hu** and D.Z. Chen, “Tissue dependent deformation field regularization through collapsed cone convolution/superposition,” *Fifty-Third Annual Meeting and Technical Exhibition of the American Association of Physicists in Medicine (AAPM)*, August 2011. *Medical Physics*, Vol. 38, No. 6, 2011.
111. L. Tang\*, S. Wang, J. Hu and **X. Hu**, “Characterizing the L1 data cache’s vulnerability to transient errors in chip-multiprocessors,” *Annual Symposium on VLSI (ISVLSI)* (IEEE), July 2011, pp. 266–271.
112. B. Zhou\*, **X. Hu** and D.Z. Chen, “Memory-efficient volume ray tracing on GPU for radiotherapy,” *IEEE Symposium on Application Specific Processors (SASP)* (IEEE), June 2011, pp. 46–51. (Nominated for the **Best Paper** Award.)
113. M. Lemmon and **X. Hu**, “Almost sure stability of networked control systems under exponentially bounded bursts of dropouts,” *International Conference on Hybrid Systems: Computation and Control (HSCC)*, April 2011, pp. 301–310.
114. S. Hong\*, **X. Hu** and M.D. Lemmon, “An adaptive transmission rate control approach to minimize energy consumption,” *IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS) – Work-in-Progress Session* (IEEE), April 2011.
115. S. Hong\*, T. Chantem\* and **X. Hu**, “Meeting end-to-end deadlines through distributed local deadline assignment,” *IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS) – Work-in-Progress Session* (IEEE), April 2011.
116. B. Zhou\*, C.X. Yu, A. Godley, X.A. Li, **X. Hu** and D.Z. Chen “Collapsed-cone based deformation field regularization for nonrigid image registration,” *IEEE International Symposium on Biomedical Imaging (ISBI)* (IEEE), March 2011, pp. 1205–1208.
117. Y. Xiang, T. Chantem\*, R. Dick, **X. Hu** and L. Shang, “System-level reliability modeling for MPSoCs,” *International Conference on Hardware/Software Co-Design and System Synthesis (CODES+ISSS)* (IEEE), October 2010, pp. 297–306.
118. J. Yi, C. Poellabauer, **X. Hu**, T. Chantem\* and L. Zhang, “Energy efficient real-time communication for wireless multihop networks,” *International Conference on Mobile Computing and Networking (Mobicom)* (refereed poster presentation), September 2010.
119. B. Zhou\*, H. Wang, C.Y. Yu, **X. Hu** and D.Z. Chen, “Optimal registration based on connected rubber model,” *Fifty-second Annual Meeting and Technical Exhibition of the American Association of Physicists in Medicine (AAPM)*, July 2010.

120. B. Zhou\*, C.Y. Yu, D.Z. Chen and **X. Hu**, “Dose calculation acceleration: a comparison study of GPU and FPGA based on collapsed cone algorithm,” *Fifty-second Annual Meeting and Technical Exhibition of the American Association of Physicists in Medicine (AAPM)*, July 2010.
121. S. Hong\*, **X. Hu** and M.D. Lemmon, “Reducing delay jitter of real-time control tasks through adaptive deadline adjustments,” *Euromicro Conference on Real-Time Systems (ECRTS)*, July 2010, pp. 229–238.
122. M. Alam, G.H. Bernstein, J. Bokor, D. Carlton, **X. Hu**, S. Kurtz\*, B. Lambson, M.T. Niemier, W. Porod, M. Siddiq and E. Varga, “Experimental progress of and prospects for nanomagnet logic (NML),” *Symposia on VLSI Technology and Circuits (IEEE)*, June 2010, pp. 1–2.
123. M. Crocker\*, **X. Hu** and M.T. Niemier, “Design and comparison of NML systolic architectures,” *International Symposium on NanoScale Architectures (NanoArch) (IEEE/ACM)*, June 2010, pp. 29–34.
124. E. Varga, M. Siddiq, M.T. Niemier, M.T. Alam, G.H. Bernstein, W. Porod, **X. Hu**, and A. Orlov, “Experimental demonstration of non-majority, nanomagnet logic gates,” *Device Research Conference (DRC)*, June 2010, pp. 87-88.
125. E. Varga, M.T. Niemier, G.H. Bernstein, W. Porod, and **X. Hu**, “Programmable nanomagnet-majority gate,” *Device Research Conference (DRC)*, June 2010, pp. 85-86.
126. E. Varga, S. Liu\*, M.T. Niemier, W. Porod, **X. Hu**, G.H. Bernstein, and A. Orlov, “Experimental demonstration of fanout for nanomagnet logic,” *Device Research Conference (DRC)*, June 2010, pp. 95-96.
127. T. Chantem\*, **X. Hu**, C. Poellabauer, J. Yi and L. Zhang, “Network-aware, energy-conscious, fair service for real-time applications on multiprocessor SoC,” *Real-Time Systems Symposium (RTSS) – Work-in-Progress Session (IEEE)*, December 2009, pp. 49–52.
128. S. Hong\*, **X. Hu** and M.D. Lemmon “An adaptive approach to reduce control delay variations,” *Real-Time Systems Symposium (RTSS) – Work-in-Progress Session (IEEE)*, December 2009, pp. 61–64.
129. M.T. Alam, M.A. Siddiq, M.T. Niemier, **X. Hu**, W. Porod and G. H. Bernstein, “Fabrication of on-chip clock structure for nanomagnet QCA (MQCA),” (*TECHCON*), 2009, pp. 206.
130. A. Dingler\*, M.J. Siddiq, M. Niemier, **X. Hu**, M. Garrison, M.T. Alam, G. Bernstein, and W. Porod, “Controlling magnetic circuits: how clock structure implementation will impact logical correctness and power,” *International Symposium on Defect and Fault Tolerance in VLSI Systems (DFTS) (IEEE)*, October 2009, pp. 94–102.
131. T. Chantem\*, **X. Hu** and R.P. Dick, “Online work maximization under a peak temperature constraint,” *International Symposium on Low Power Electronics and Design (ISLPED) (ACM/IEEE)*, August 2009, pp. 105–110.



132. A. Dingler\*, M. Niemier, **X. Hu**, M. Garrison and M. Alam, "System-level energy and performance projections for nanomagnet-based logic," *International Symposium on Nanoscale Architectures (NanoArch)* (ACM/IEEE), August 2009, pp. 21–26. (Received the **Best Paper** Award.)
133. B. Zhou\*, **X. Hu**, D.Z. Chen and C.X. Yu, "A multi-FPGA hardware accelerator for dose calculation in cancer treatment," *IEEE Symposium on Application Specific Processors (SASP)* (IEEE), Aug 2009, pp. 70–79.
134. B. Zhou\*, **X. Hu**, D.Z. Chen and C.X. Yu, "A multi-FPGA accelerator for dose calculation in radiation therapy," *Fifty-first Annual Meeting and Technical Exhibition of the American Association of Physicists in Medicine (AAPM)*, July 2009. *Medical Physics*, Vol. 36, No. 6, 2009.
135. B. Zhou\*, **X. Hu**, D.Z. Chen and C.X. Yu, "GPU-based implementation of Monte Carlo superposition for dose calculation," *Fifty-first Annual Meeting and Technical Exhibition of the American Association of Physicists in Medicine (AAPM)*, July 2009. *Medical Physics*, Vol. 36, No. 6, 2009.
136. J. Yi, C. Poellabauer, **X. Hu**, J. Simmer\* and L. Zhang, "Energy-conscious co-scheduling of tasks and packets in wireless real-time environments," *Real-Time and Embedded Technology and Applications Symposium (RTAS)* (IEEE), April 2009, pp. 265–274.
137. E. Varga, M. Niemier, G. Bernstein, W. Porod and **X. Hu**, "Non-volatile and reprogrammable MCQA-based majority gates," *Device Research Conference (DRC)*, June 2009.
138. Y. Yu, S. Ren and **X. Hu**, "A metric for judicious relaxation of timing constraints in soft real-time systems," *Real-Time and Embedded Technology and Applications Symposium (RTAS)* (IEEE), April 2009, pp. 163–172.
139. D.R. Bild, S. Misra, T. Chantem\*, P. Kumar, R.P. Dick, **X. Hu**, L. Shang and A. Choudhary, "Temperature-aware test scheduling for multiprocessor systems-on-chip," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2008, pp. 59–66
140. M.T. Niemier, A.J. Dingler\* and **X. Hu**, "Bridging the gap between nanomagnetic devices and circuits," *International Conference on Computer Design (ICCD)* (IEEE), October 2008, pp. 506–513.
141. D. Rajan, C. Poellabauer, **X. Hu**, L. Zhang and K. Otten\*, "Wireless channel access reservation for embedded real-time systems," *International Conference on Embedded Software (EMSOFT)* (ACM/IEEE), October 2008, pp. 129–138.
142. M.T. Niemier, M. Crocker\* and **X. Hu**, "Fabrication variations and defect tolerance for nanomagnet-based QCA", *International Symposium on Defect and Fault Tolerance in VLSI Systems (DFTS)* (IEEE), October 2008, pp. 534–542.
143. M.T. Niemier, A.J. Dingler\* and **X. Hu**, "Design tradeoffs for improved performance in magnetic QCA-based systems," *International Workshop on Design and Test of Nano Devices, Circuits and Systems (NDCS)* (IEEE), September 2008, pp. 35–38.

144. T. Chantem\*, X. Wang, M.D. Lemmon and **X. Hu**, "Period and deadline selection for schedulability in real-time systems," *Euromicro Conference on Real-Time Systems (ECRTS)*, July 2008, pp. 181–190.
145. M. Crocker\*, **X. Hu** and M.T. Niemier, "Defect tolerance in QCA-based PLAs," *International Symposium on NanoScale Architectures (NanoArch)* ACM/(IEEE), June 2008, pp. 46–53.
146. T. Chantem\*, R. Dick and **X. Hu**, "Temperature-aware scheduling and assignment for hard real-time applications on MPSoCs," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2008, pp. 288–293.
147. M.T. Alam, G.H. Bernstein, W. Porod, **X. Hu**, M. Niemier, M. Putney and J. DeAngelis\*, "Power dissipation for clocked magnetic QCA," *International Workshop on Computational Electronics*, October 2007.
148. M. Crocker\*, **X. Hu** and M.T. Niemier, "Fault models and yield analysis for QCA-based PLAs," *International Conference on Field Programmable Logic and Applications (FPL)* (IEEE), August 2007, pp. 435–440.
149. M.T. Niemier, **X. Hu**, M.T. Alam, G.H. Bernstein, W. Porod, M. Putney and J. DeAngelis\*, "Clocking structures and power analysis for nanomagnet-based logic devices," *International Symposium on Low Power Electronics and Design (ISLPED)* (ACM/IEEE), August 2007, pp. 26–31.
150. M.T. Alam, J. DeAngelis\*, M. Putney, **X. Hu**, W. Porod, M.T. Niemier and G.H. Bernstein, "Clocking scheme for nanomagnet QCA," *IEEE International Conference on Nanotechnology (IEEE-NANO)* (IEEE), August 2007, pp. 403–408.
151. A. Chaudhary, D.Z. Chen, R. Fleischer, **X. Hu**, J. Li, M.T. Niemier, Z. Xie and H. Zhu, "Approximating the maximum sharing problem," *Lecture Notes in Computer Science*, Vol. 4619, Springer Verlag, *Proc. of the 10th Workshop on Algorithms and Data Structures (WADS)*, August 2007, pp. 52–63.
152. G. Bernstein, M. Alam, W. Porod, **X. Hu**, M. Niemier, M. Putney and J. DeAngelis\*, "Clocking scheme for nanomagnet QCA (NMQCA)," *IEEE International Conference on Nanotechnology (IEEE-NANO)* (IEEE), August 2007.
153. B. Zhou\*, **X. Hu**, D.Z. Chen and C.X. Yu, "Hardware acceleration for 3-D radiation dose calculation," *IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP)* (IEEE), July 2007, pp. 290–295.
154. M.T. Alam, M.T. Niemier, W. Porod, **X. Hu**, M. Putney, J. DeAngelis\* and G.H. Bernstein, "On-Chip Clocking Scheme for Nanomagnet QCA," *Device Research Conference (DRC)*, June 2007, pp. 133–134.
155. M. Lemmon, T. Chantem\*, **X. Hu** and M. Zyskowski, "On self-triggered full information H-infinity controllers," *International Conference on Hybrid Systems: Computation and Control (HSCC)*, April 2007, pp. 371–384.

156. B. Mochocki\*, D. Rajan, **X. Hu**, C. Poellabauer, K. Otten\* and T. Chantem\*, “Network-aware dynamic voltage and frequency scaling,” *Real-Time and Embedded Technology and Applications Symposium (RTAS)* (IEEE), April 2007, pp. 215–224.
157. T. Chantem\*, **X. Hu** and M. Lemmon, “Generalized elastic scheduling,” *Real-Time Systems Symposium (RTSS)* (IEEE), December 2006, pp. 236–245.
158. D.Z. Chen, **X. Hu**, S. Luan, E. Misiolek and C. Wang, “Shape rectangularization problems in intensity-modulated radiation therapy,” *International Symposium on Algorithms and Computation (ISAAC)*, 2006, December 2006, pp. 701–711.
159. M.T. Niemier, M. Crocker\*, **X. Hu** and M. Lieberman, “Using CAD to shape experiments in molecular QCA,” *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2006, pp. 907–914.
160. R. Racu, R. Ernst, A. Hamann, B. Mochocki\* and **X. Hu**, “Methods for power optimization in distributed embedded systems with real-time requirements,” *International Conference on Compilers, Architecture, and Synthesis for Embedded Systems (CASES)* (ACM/IEEE), October 2006, pp. 379–388.
161. B. Mochocki\*, K. Lahiri, S. Cadambi and **X. Hu**, “Signature-based workload estimation for mobile 3D graphics,” *Design Automation Conference (DAC)* (ACM/IEEE), July 2006, pp. 592–597.
162. D.Z. Chen, **X. Hu**, S. Luan and C. Wang, “A leaf sequencing software for intensity-modulated radiation therapy,” *19th IEEE Symposium on Computer-Based Medical Systems (CBMS)* (IEEE), June 2006, pp. 3–8.
163. M.T. Niemier, **X. Hu**, M. Lieberman and M. Crocker\*, “Using DNA as a circuit board for a molecular QCA PLA,” *Foundations of Nanoscience (FNANO)*, April 2006, pp. 96–107.
164. **X. Hu**, T. Chantem\* and M. Lemmon, “Optimal elastic scheduling,” *Real-Time and Embedded Technology and Applications Symposium (RTAS) – Work-in-Progress Session* (IEEE), April 2006, pp. 13–20.
165. K. Whitton\*, **X. Hu**, C.Y. Yu and D.Z. Chen, “An FPGA solution for radiation dose calculation,” *IEEE Symposium on Field-Programmable Custom Computing Machines (FCCM)* (IEEE), April 2006, pp. 227–236.
166. **X. Hu**, M. Crocker\*, M.T. Niemier, M. Yan and G.H. Bernstein, “PLAs in Quantum-dot Cellular Automata,” *Annual Symposium on VLSI (ISVLSI)* (IEEE), March 2006, pp. 242–247.
167. B. Mochocki\*, **X. Hu**, R. Racu and R. Ernst, “Dynamic voltage scaling for the schedulability of jitter-constrained real-time embedded systems,” *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2005, pp. 446–449.
168. A. Chaudhary, D.Z. Chen, **X. Hu**, K. Whitton\*, M.T. Niemier and R. Ravichandran, “Eliminating wire crossings for molecular Quantum-dot Cellular Automata implementation,” *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2005, pp. 565–571.

169. D. Liu\*, **X. Hu**, M. Lemmon and Q. Ling, "Scheduling tasks with Markov-Chain constraints," *Euromicro Conference on Real-Time Systems (ECRTS)*, July 2005, pp. 157–166.
170. D.Z. Chen, **X. Hu**, S. Luan, C. Wang and X. Wu, "Mountain reduction, block matching, and applications in intensity-modulated radiation therapy," *ACM Symposium on Computational Geometry (SCG)* (ACM), June 2005, pp. 35–44.
171. B. Mochocki\*, **X. Hu** and G. Quan\*, "Practical on-line DVS scheduling for fixed-priority real-time systems," *IEEE Real-time Technology and Applications Symposium (RTAS)* (IEEE), March 2005, pp. 224–233.
172. L. Leung, C.-Y. Tsui and **X. Hu**, "Exploiting dynamic workload variation in low energy preemptive task scheduling," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2005, pp. 634–639.
173. P. Kalla\*, **X. Hu** and J. Henkel, "A flexible framework for communication evaluation in SoC design," *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2005, pp. 956–959.
174. G. Quan\*, L. Niu, **X. Hu** and B. Mochocki\*, "Fixed priority scheduling for reducing overall energy on variable voltage processors," *Real-time Systems Symposium (RTSS)* (IEEE), December 2004, pp. 309–318.
175. D.Z. Chen, **X. Hu** S. Luan, C. Wang, S.A. Naqvi and C.X. Yu, "Generalized Geometric Approaches for Leaf Sequencing Problems in Radiation Therapy," *Lecture Notes in Computer Science*, Vol. 3341, Springer Verlag, *Proc. of 15th Annual International Symposium on Algorithms and Computation (ISAAC)*, December 2004, pp. 271–281.
176. L. Leung, C.-Y. Tsui and **X. Hu** "Exploiting dynamic workload variation in offline low energy voltage scheduling," *International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS)* (IEEE), September 2004, *Lecture Notes in Computer Science*, Vol. 3254, September 2004, pp. 553–563.
177. S. Luan, C. Wang, D.Z. Chen, **X. Hu**, S.A. Naqvi and C.X. Yu, "A new MLC segmentation algorithm for step-and-shoot IMRT without tongue-and-groove leakage," *Forty-sixth Annual Meeting and Technical Exhibition of the American Association of Physicists in Medicine (AAPM)*, 2004. *Medical Physics*, Vol. 31, No. 6, June 2004.
178. S. Luan, C. Wang, D.Z. Chen, **X. Hu** and C.X. Yu, "A study of the impact of MLC constraints on the number of segments in step-and-shoot IMRT delivery," *Forty-sixth Annual Meeting and Technical Exhibition of the American Association of Physicists in Medicine (AAPM)*, 2004. *Medical Physics*, Vol. 31, No. 6, June 2004.
179. D.A. Antonelli\*, D.Z. Chen, T.J. Dysart, **X. Hu**, A. Kahng, P.M. Kogge, R.C. Murphy and M.T. Niemier, "Quantum-Dot Cellular Automata (QCA) circuit partitioning: problem modeling and solutions," *Design Automation Conference (DAC)* (ACM/IEEE), June 2004, pp. 363–368.
180. Z. Wang\* and **X. Hu**, "Power aware variable partitioning and instruction scheduling for multiple memory banks," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), February 2004, pp. 312–317.

181. D. Liu\*, **X. Hu**, M. Lemmon and Q. Ling, "Firm real-time system scheduling based on a novel QoS constraint," *Real-time Systems Symposium (RTSS)* (IEEE), December 2003, pp. 386–395.
182. P. Kalla\*, **X. Hu** and J. Henkel, "LRU-SEQ: A novel replacement policy for leakage energy reduction in instruction caches," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2003, pp. 518–522.
183. D.Z. Chen, **X. Hu**, S. Luan, C. Wang, S.A. Naqvi, C.F. Lee and C.X. Yu, "A new leaf sequencing algorithm/software for step and shoot IMRT delivery," *Forty-fifth Annual Meeting and Technical Exhibition of the American Association of Physicists in Medicine (AAPM)*, 2003. *Medical Physics*, Vol. 30, No. 6, June 2003, p. 1404.
184. D.Z. Chen, **X. Hu**, S. Luan, C. Wang and X. Wu, "Geometric algorithms for static leaf sequencing problems in radiation therapy," *ACM Symposium on Computational Geometry (SCG)* (ACM), June 2003, pp. 88–97.
185. P. Kalla\*, **X. Hu**, and J. Henkel, "SEA: Fast Power Estimation for Micro-Architectures," *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2003, pp. 600–605.
186. Z. Wang\*, **X. Hu** and E. Sha, "Register aware scheduling for distributed cache clustered architecture," *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2003, pp. 71–76.
187. Y. Zhang\*, **X. Hu** and D.Z. Chen, "Energy minimization of real-time tasks on variable voltage processors with transition energy overhead," *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2003, pp. 65–70.
188. B. Mochocki\*, **X. Hu** and G. Quan\*, "A realistic variable voltage scheduling model for real-time applications," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2002, pp. 726–731.
189. D.Z. Chen, **X. Hu**, S. Luan, X. Wu and C.X. Yu, "Optimal terrain construction problems and applications in intensity-modulated radiation therapy," *Lecture Notes in Computer Science*, Vol. 2461, Springer Verlag, *Proc. of the Tenth Annual European Symposium on Algorithms (ESA)*, September 2002, pp. 270–283.
190. Y. Zhang\*, **X. Hu** and D.Z. Chen, "Task scheduling and voltage selection for energy minimization," *Design Automation Conference (DAC)* (ACM/IEEE), June 2002, pp. 183–188.
191. G. Quan\* and **X. Hu**, "Minimum energy fixed-priority scheduling for variable voltage processors," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2002, pp. 782–787.
192. H. Liu\* and **X. Hu**, "Efficient performance estimation for general real-time task systems," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2001, pp. 464–470.

193. Z. Wang\*, E.H.-M. Sha and **X. Hu**, “Combining partitioning and data padding for scheduling multiple loop nests,” *International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)*, November 2001, pp. 67–75.
194. D.Z. Chen, **X. Hu** and X. Wu, “Maximum red/blue interval matching with applications,” *Seventh Annual International Computing and Combinatorics Conference (COCOON)*, August 2001, pp. 150–158.
195. X. Wu, D.Z. Chen, **X. Hu**, S. Luan, L. Zhang and C.X. Yu, “A new leaf-sequencing algorithm for intensity-modulated arc therapy,” *Forty-Third Annual Meeting and Technical Exhibition of the American Association of Physicists in Medicine (AAPM)*, July 2001, pp. 1252.
196. D.Z. Chen, **X. Hu**, Y. Huang, Y. Li, and J. Xu, “Algorithms for congruent sphere packing and applications,” *Seventeenth Annual ACM Symposium on Computational Geometry (SCG)* (ACM), June 2001, pp. 212–221.
197. G. Quan\* and **X. Hu**, “Energy efficient fixed-priority scheduling for real-time systems on variable voltage processors,” *Design Automation Conference (DAC)* (ACM/IEEE), June 2001, pp. 828–833. (Received the **Best Paper Award**.)
198. B. Hanounik\* and **X. Hu**, “Linear-time matrix transpose algorithms using vector register file with diagonal registers,” *International Parallel and Distributed Processing Symposium (IPDPS)* (IEEE), April 2001, pp. 35 (6 pages).
199. Y. Zhang\*, **X. Hu** and D.Z. Chen, “Cell selection from technology libraries for minimizing power,” *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), February 2001, pp. 609–614.
200. G. Quan\* and **X. Hu**, “Enhanced Fixed-Priority Scheduling with (m,k)-Firm Guarantee,” *Real-Time Systems Symposium (RTSS)* (IEEE), December 2000, pp. 79–88.
201. D.Z. Chen, **X. Hu** and J. Xu, “Optimal beam penetrations in two and three dimensions,” *Lecture Notes in Computer Science, Vol. 1969*, Springer Verlag, *International Symposium on Algorithms and Computation (ISAAC)*, December 2000, pp. 491–502.
202. D.Z. Chen, **X. Hu**, and X. Wu, “Optimal polygon cover problems and applications,” *Lecture Notes in Computer Science, Vol. 1969*, Springer Verlag, *International Symposium on Algorithms and Computation (ISAAC)*, December 2000, pp. 564–576.
203. G. Greenwood, **X. Hu** and S. Ravichandran, “Modeling epistatic interactions in fitness landscapes,” *Congress on Evolutionary Computation* (IEEE), July 2000, pp. 932–938.
204. G. Quan\* and **X. Hu**, “Fast performance prediction for periodic task systems,” *International Workshop on Hardware-Software Codesign (CODES)* (ACM/IEEE), May 2000, pp. 72–76.
205. C. Chantrapornchai, E.H.-M. Sha and **X. Hu**, “A novel approach to module selection,” with C. Chantrapornchai and E.H.-M. Sha, *10th Great Lakes Symposium on VLSI (GLVLSI)* (IEEE), March 2000, pp. 139–142.

206. G. Quan\*, **X. Hu** and G.W. Greenwood, "Preference-driven hierarchical hardware/software partitioning," *International Conference on Computer Design (ICCD)* (IEEE), October 1999, pp. 652–657.
207. D.Z. Chen, **X. Hu** and J. Xu, "Optimal beam penetrations in two and three dimensions," presented at the *4th CGC Workshop on Computational Geometry*, October 1999.
208. Y. Zhang\*, **X. Hu** and D.Z. Chen, "Global register allocation for minimizing energy consumption," *International Symposium on Lower Power Electronics and Design (ISLPED)* (ACM/IEEE), August 1999, pp. 100–102.
209. **X. Hu**, G.W. Greenwood, S. Ravichandran and G. Quan\*, "A framework for user assisted design exploration," *Design Automation Conference (DAC)* (ACM/IEEE), June 1999, pp. 414–419.
210. D.Z. Chen, O. Daescu, **X. Hu**, X. Wu and J. Xu, "Determining an optimal penetration among weighted regions in two and three dimensions," *ACM Symposium on Computational Geometry (SCG)* (ACM), June 1999, pp. 322–331.
211. T. Zhou\*, **X. Hu** and E.H.-M. Sha, "A probabilistic performance metric for real-time system design," *7th International Workshop on Hardware-Software Codesign (CODES)* (ACM/IEEE), May 1999, pp. 90–94.
212. Y. Zhang\*, **X. Hu** and D.Z. Chen, "Low energy register allocation beyond basic blocks," *International Symposium on Circuits and Systems (ISCAS)* (IEEE), June 1999, pp. 290–293.
213. T. Zhou\*, **X. Hu** and E.H.-M. Sha, "Probabilistic performance estimation for real-time embedded systems," *International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems (TAU)* (ACM/IEEE), March 1999, pp. 83–88.
214. C. Chantrapornchai, E.H.-M. Sha and **X. Hu**, "Efficient algorithms for finding highly acceptable designs based on module-utility selections," *9th Great Lakes Symposium on VLSI (GLVLSI)* (IEEE), March 1999, pp. 128–131.
215. **X. Hu** and M.L. Benson\*, "Design CORDIC-based systems using term-rewriting techniques," *41st Midwest Symposium of Circuits and Systems (MSCAS)* (IEEE), August 1998, pp. 288–291.
216. C. Chantrapornchai, E.H.-M. Sha and **X. Hu**, "Efficient scheduling for imprecise timing based on fuzzy theory," *41st Midwest Symposium of Circuits and Systems (MSCAS)* (IEEE), August 1998, pp. 272–275.
217. D.Z. Chen, O. Daescu, **X. Hu** and J. Xu, "Finding an optimal path without growing the tree," *Lecture Notes in Computer Science, Vol. 1461*, Springer Verlag, *Sixth Annual European Symposium on Algorithms (ESA)*, August 1998, pp. 356–367.
218. C. Chantrapornchai, S. Tongshima, E. H.-M. Sha and **X. Hu**, "Dealing with impreciseness in architectural synthesis," *International Conference on Artificial Intelligence and Soft Computing (IASTED)*, May 1998, pp. 473–476.

219. J.J. Brown, D.Z. Chen, G.W. Greenwood, **X. Hu** and R.W. Taylor, "Scheduling for power reduction in a real-time system," *International Symposium on Lower Power Electronics and Design (ISLPED)* (IEEE), August 1997, pp. 84–87.
220. R. Sambandam\* and **X. Hu**, "Predicting timing behavior in architectural design exploration of real-time embedded systems," *Design Automation Conference (DAC)*, (ACM/IEEE), June 1997, pp. 157–160.
221. **X. Hu**, G.W. Greenwood and J.G. D'Ambrosio, "An evolutionary approach to configuration-level hardware/software partitioning," *Fourth International Conference on Parallel Problem Solving from Nature (PPSN)*, September 1996, pp. 900–909.
222. D.Z. Chen and **X. Hu**, "Efficient approximation algorithms for floorplan area minimization," *Design Automation Conference (DAC)*, (ACM/IEEE), June 1996, pp. 483–486.
223. D.Z. Chen, **X. Hu** and P.J. Blatner, "Efficient algorithms for orthogonal polygon approximation," *International Symposium on Circuits and Systems (ISCAS)* (IEEE), May 1996, Vol. 4, pp. 779–782.
224. T.F. Piatkowski, G.W. Greenwood, J. Grantner, **X. Hu** and R.W. Taylor, "Curriculum proposal for an innovative BS/MS in computer engineering emphasizing real-time embedded systems," *IEEE Workshop on Real-Time Systems Education* (IEEE), April 1996, pp. 54–62.
225. J.G. D'Ambrosio and **X. Hu**, "Configuration-level hardware/software partitioning for real-time embedded systems," *Third International Workshop on Hardware-Software Co-Design (CODES)* (IEEE), September 1994, pp. 34–41.
226. D.Z. Chen and **X. Hu**, "Fast and efficient operations on parallel priority queues," *Lecture Notes in Computer Science, No. 834: International Symposium on Algorithms and Computation (ISAAC)*, August 1994, pp. 279–287.
227. J.G. D'Ambrosio, **X. Hu**, B.T. Murray and D. Tang, "The role of analysis in hardware/software co-design," *Second International Workshop on Hardware-Software Co-Design (CODES)* (IEEE), October 1993.
228. **X. Hu** and S.C. Bass, "A neglected error source in the CORDIC algorithm," *International Symposium on Circuits and Systems (ISCAS)* (IEEE), May 1993, pp. 766–769.
229. **X. Hu**, R.G. Harber and S.C. Bass, "Minimizing the number of delay buffers in the synchronization of pipelined systems," *Design Automation Conference (DAC)* (ACM/IEEE), June 1991, pp. 758–763.
230. R.G. Harber, **X. Hu** and S.C. Bass, "Maximal solution of linear systems of equations and an application in VLSI," *International Symposium on Circuits and Systems (ISCAS)* (IEEE), Vol. 3, May 1990, pp. 2337–2340.
231. R.G. Harber, **X. Hu**, J. Li and S.C. Bass, "Bit-serial CORDIC circuits for use in a VLSI silicon compiler," *International Symposium on Circuits and Systems (ISCAS)* (IEEE), Vol. 1, May 1989, pp. 154–157.



232. **X. Hu**, R.G. Harber, J. Li and S.C. Bass, “The application of bit-serial CORDIC computational units to the design of inverse kinematics processors,” with R.G. Harber, J. Li and S.C. Bass, *International Conference on Robotics and Automation (ICRA)* (IEEE), Vol. 2, May 1988, pp. 1152–1157.

### Invited and Other Publications

1. R. Ernst and **X. Hu**, “Autonomous systems design — a virtual roundtable,” *IEEE Computer*, Vol. 54, No. 11, pp. 17–25, November 2021.
2. X. Guo, S. Han, **X. Hu**, X. Jiao, Y. Jin, F. Kong and M. Lemmon, “Towards scalable, secure, and smart mission-critical IoT systems: review and vision: (Special Session Paper),” *International Conference on Embedded Software* (ACM/IEEE), October 2021, pp. 1–10.
3. **X. Hu**, M. Niemier, A. Kazemi\*, A. F. Laguna\*, K. Ni, R. Rajaei\*, M. M. Sharifi\* and X. Yin, “In-memory computing with associative memories: a cross-layer perspective,” an **invited** paper, *IEEE International Electron Devices Meeting* (IEEE), December 2021.
4. H. Amrouch, D. Gao , **X. Hu**, A. Kazemi\*, A. F. Laguna\*, K. Ni, M. Niemier, M. M. Sharifi\*, S. Thomann, X. Yin and C. Zhuo, “ICCAD tutorial session paper: Ferroelectric FET technology and applications: from devices to systems,” *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2021.
5. D. Reis\*, A.F. Laguna\*, A. M. Niemier and **X. Hu**, “Exploiting FeFETs via cross-layer design from in-memory computing circuits to meta-learning applications,” an **invited** paper, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), 2021, pp. 306–311.
6. H. Amrouch, **X. Hu**, M. Imani, A. Laguna\*, M. Niemier, S. Thomann, X. Yin\* and C. Zhuo, “Cross-layer design for Computing-in-Memory: From Devices,Circuits, to Architectures and Applications,” an **invited** paper, *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2021, pp. 132–139.
7. Z. Yan\*, D.-C. Juan, **X. Hu** and Y. Shi, “Uncertainty modeling of emerging device based computing-in-memory neural accelerators with application to neural architecture search,” an **invited** paper, *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2021, pp. 859–864.
8. D. Ma, X. Yin\*, M. Niemier, **X. Hu** and X. Jiao, “AxR-NN: Approximate computation reuse for energy-efficient convolutional neural networks,” an **invited** paper, *Great Lakes VLSI Symposium (GLVLSI)* (ACM), September 2020, pp. 363–368.
9. D. Reis\*, D. Gao, X. Yin, D. Fan, M. Niemier, C. Zhuo and **X. Hu**, “Modeling and benchmarking computing-in-memory for design space exploration,” an **invited** paper, *Great Lakes VLSI Symposium (GLVLSI)* (ACM), September 2020, pp. 39–44.
10. Z. Zhu, H. Sun, K. Qiu, L. Xia, G. Krishnan, G. Dai, D. Niu, X. Chen, **X. Hu**, Y. Cao, Y. Xie, Y. Wang and H. Yang, “MNSIM 2.0: A behavior-level modeling tool for memristor-based neuromorphic computing systems,” an **invited** paper, *Great Lakes VLSI Symposium (GLVLSI)* (ACM), September 2020, pp. 83–88.

11. D. Brooks, T. Gokmen, U. Gupta, **X. Hu**, S. Jain, A.F. Laguna\*, M. Niemier, A. Raghunathan, A. Ranjan, D. Reis\*, J. Stevens, C-J. Wu and X. Yin\*, “Emerging neural workloads and their impact on hardware,” an **invited** paper, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2020, pp. 1462–1471.
12. J. Henkel, H. Amrouch, M. Rapp, S. Salamin, D. Reis\*, D. Gao, X. Yin\*, M. Niemier, C. Zhuo, **X. Hu**, H.-Y. Cheng, C.-L. Yang, “The impact of emerging technologies on architectures and system-level management,” an **invited** paper, *International Conference on Computer-Aided Design (ICCAD)* (ACM/IEEE), November 2019, pp. 794–799.
13. S. Angizi, Z. He, D. Reis\*, **X. Hu**, W. Tsai, S. J. Lin and D. Fan, “Accelerating deep neural networks in processing-in-memory platforms: analog or digital approach?” an **invited** paper, *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)* (IEEE), 2019, pp. 197–202.
14. X. Yin\*, D. Reis\*, M. Niemier and **X. Hu**, “Ferroelectric FET based TCAM designs for energy efficient computing” an **invited** paper, *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)* (IEEE), July 2019, pp. 437–442.
15. A.F. Laguna\*, X. Yin\*, D. Reis\*, M. Niemier and **X. Hu**, “Ferroelectric FET based In-memory computing,” an **invited** paper, *Great Lakes VLSI Symposium (GLVLSI)* (ACM), May 2019, pp. 373–378.
16. **X. Hu**, R. Ernst, P. Eles, G. Heiser, K. Keutzer, D. Kim and T. Tohdo, “Roundtable: Machine learning for embedded systems: hype or lasting impact?” *IEEE Design & Test*, Vol. 35, No. 6, pp. 86–93, 2018.
17. S. Rai, S. Srinivasa, P. Cadareanu, X. Yin\*, **X. Hu**, P.-E. Gaillardon, V. Narayanan and A. Kumar, “Emerging reconfigurable nanotechnologies: can they support future electronics?” an **invited** paper, *International Conference on Computer-Aided Design (ICCAD)* (ACM/IEEE), November 2018, Article 13, 8 pages.
18. A. Aziz, E.T. Breyer, A. Chen, X. Chen\*, S. Datta, S.K. Gupta, M. Hoffmann, **X. Hu**, A. Ionescu, M. Jerry, T. Mikolajick, H. Mulaosmanovic, K. Ni, M. Niemier, I. O’Connor, A. Saha, S. Slesazek, S.K. Thirumala and X. Yin\*, “Computing with ferroelectric FETs: Devices, models, systems, and applications,” an **invited** paper, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2018, pp. 1295–1304.
19. X. Yin\*, Z. Toroczkai and **X. Hu**, “An analog SAT solver based on a deterministic dynamical system,” an **invited** paper, *International Conference on Computer-Aided Design (ICCAD)* (ACM/IEEE), November 2017, pp. 794–799.
20. X. Xu, Q. Lu, T. Wang, J. Liu, C. Zhuo, **X. Hu** and Y. Shi, “Edge Segmentation: Empowering mobile telemedicine with compressed cellular neural networks,” an **invited** paper, *International Conference on Computer-Aided Design (ICCAD)* (ACM/IEEE), November 2017, pp. 880–887.
21. R. Perricone\*, M. Niemier, and **X. Hu**, an **invited** paper, “Challenges and opportunities with spin-based logic,” *SPIE 10357, Spintronics X*, 2017, pp. 103570M.

22. J.-P. Wang, S. S. Sapatnekar, C. H. Kim, P. Crowell, S. Koester, S. Datta, K. Roy, A. Raghunathan, **X. Hu**, M. Niemier, A. Naeemi, C.-L. Chien, C. Ross and R. Kawakami, "A pathway to enable exponential scaling for the beyond-CMOS era," an **invited** paper, *Design Automation Conference (DAC)* (ACM/IEEE), June 2017, Article 16, 6 pages.
23. R. Perricone\*, L. Tang\*, M. Niemier and **X. Hu**, "Exploiting non-volatility for information processing," an **invited** paper, *Great Lakes VLSI Symposium (GLVLSI)* (ACM), May 2017, pp. 305–310.
24. A. Horvath, M. Hillmer, Q. Lou\*, **X. Hu** and M. Niemier, "Cellular neural network friendly convolutional neural networks – CNNs with CNNs," an **invited** paper, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2017, pp. 145-150.
25. R. Perricone\*, I. Ahmed, Z. Liang, M.G. Mankalaley **X. Hu**, C. H. Kim, M.Niemier, S.S. Sapatnekar and J-P Wang, "Advanced spintronic memory and logic for non-volatile processors," an **invited** paper, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2017, pp. 972-977.
26. J. Wu, J. Liu, **X. Hu** and Y. Shi, "Privacy protection via appliance scheduling in smart homes," an **invited** paper, *International Conference on Computer-Aided Design (ICCAD)* (ACM/IEEE), November 2016, pp. 106–111.
27. S. Hu, **X. Hu** and A. Zomaya, "Leveraging design automation techniques for cyber-physical system design," **Guest Editorial**, *IEEE Transactions on CAD of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 35, No 5, 2016, pp. 697–698.
28. A. Chen, **X. Hu**, Y. Jin, M. Niemier and X. Yin\*, "Enhancing hardware security with emerging transistor technologies," an **invited** paper, *ACM Great Lakes Symposium on VLSI (GLVLSI)* (ACM), May 2016, pp. 305–310.
29. R. Perricone\*, **X. Hu**, J. Nahas, and M. Niemier, "Can beyond-CMOS devices illuminate dark silicon?" an **invited** paper, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2016, pp. 13–18.
30. A. Chen, **X. Hu**, Y. Jin, M. Niemier and X. Yin\*, "Using emerging technologies for hardware security beyond PUFs," an **invited** paper, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2016, pp. 1544–1549.
31. M.T. Niemier and **X. Hu**, "Potential benefits from image processing hardware based on emerging transistor technologies," an **invited** paper, *International Society for Optics and Photonics (SPIE) Newsroom*, June 2015.
32. I. Palit\*, Q. Lou\*, M.T. Niemier, B. Sedighi\*, J.J. Nahas and **X. Hu**, "Cellular neural networks for image analysis using steep slope devices," an **invited** paper, *International Conference on Computer-Aided Design (ICCAD)* (ACM/IEEE), November 2014, pp. 92–95.
33. N. Chandramoorthy, V.Narayanan, K. Swaminathan, M. Cotter, X. Li, I. Palit\*, **X. Hu**, M.T. Niemier, K.M. Irick, "Understanding the landscape of accelerators for vision," *IEEE Workshop on Signal Processing Systems (SiPS)* (IEEE), October 2014, pp. 280–285.

34. G.H. Bernstein, K. Butler, P. Li, F. Shah, M. Siddiq, G. Csaba, **X. Hu**, M.T. Niemier, and W. Porod, "Nanomagnet logic – from concept to prototype," an **invited** paper, *Tech-Connect World, Innovation Conference & Expo*, June 2014, pp. 61–64.
35. I. Palit\*, B. Sedighi\*, A. Horvath, **X. Hu**, J.J. Nahas and M T. Niemier, "Impact of steep-slope transistors on non-von Neumann architectures: CNN case study," an **invited** paper, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2014, pp. 1–6.
36. I. Palit\*, **X. Hu**, J.J. Nahas and M T. Niemier, "TFET based cellular neural network architectures," an **invited** paper, *International Symposium on Low Power Electronics and Design (ISLPED)* (ACM/IEEE), September 2013, pp. 236–241.
37. J.-J. Chen, J. Henkel and **X. Hu**, "Guest Editorial: Special Section on Power-Aware Design for Embedded Systems," *IEEE Transactions on Industrial Informatics (IEEE TII)*, Vol. 9, No. 1, 2013, pp. 485-486.
38. R. Barrett, S. Dosanjh, M. Heroux, **X. Hu**, S. Parker and J. Shalf, "Toward codesign in high performance computing systems," an **invited** paper, *International Conference on Computer-Aided Design (ICCAD)* (ACM/IEEE), 2012, pp. 443–449.
39. W. Porod, P. Li, F. Shah, M. Siddiq, E. Varga, G. Csaba, V. Sankar, G.H. Bernstein, **X. Hu**, M.T. Niemier, J. Nahas and A. Orlov, an **invited** paper, "Nanomagnet logic," *Device Research Conference (DRC)*, June, 2012, pp. 213–214.
40. G.H. Bernstein, P. Li, F. Shah, M. Siddiq, E. Varga, V. Sankar, G. Csaba, **X. Hu**, M. Niemier, J. Nahas, A. Orlov, and W. Porod, "Nanomagnet logic: a new paradigm in low-power computing systems," an **invited** paper, *Annual Conference Foundations of Nanoscience (FNANO12)*, 2012.
41. **X. Hu**, R.C. Murphy, S.S. Dosanjh, K. Olukotun and S. Poole, "Hardware/software co-design for high performance computing: challenges and opportunities," an **invited** paper, *International Conference on Hardware/Software Co-Design and System Synthesis (CODES+ISSS)* (IEEE), 2010.
42. S. Kurtz\*, M. Niemier, **X. Hu**, W. Porod and G.H. Bernstein, "Design space exploration for nanomagnet logic systems," an **invited** paper, *Foundations of Nanoscience (FNANO)*, April, 2010, pp. 62–63.
43. T. Chantem\*, **X. Hu**, C. Poellabauer, J. Yi and L. Zhang, " Network-aware, energy-conscious, fair service for real-time applications on multiprocessor SoC," an **invited** paper, *ACM SIGBED Review*, Vol. 7, No. 1, January 2010, Article No. 2.
44. M.T. Alam, S. Kurtz\*, M.T. Niemier, **X. Hu**, G.H. Bernstein, and W. Porod, "Magnetic logic based on field-coupled nanomagnets: clocking structures and power analysis," an **invited** paper, *Foundations of Nanoscience (FNANO)*, April 2009.
45. **X. Hu**, A. Khitun, K.K. Likharev, M.T. Niemier, M.B. Bao and K.L. Wang, "Design and defect tolerance beyond CMOS," an **invited** paper, *International Conference on Hardware/Software Co-Design and System Synthesis (CODES+ISSS)* (IEEE), October 2008, pp. 223–229.

46. J. Henkel, **X. Hu** and S. S. Bhattacharyya, "Guest Editors' Introduction: Taking on the embedded system design challenge," *IEEE Computer*, Vol. 36, No. 4, 2003, pp. 35-37.
47. P. Kalla, **X. Hu** and J. Henkel, "SEA: Fast power estimation for micro-architectures," an **invited** paper, *International Conference on ASIC (ASICON)*, October 2003, pp. 1200.
48. J.G. D'Ambrosio, **X. Hu**, B.T. Murray and D. Tang, "Techniques for analyzing PCM systems," *GM Internal Research Report*, E3-314, September 1992.
49. **X. Hu**, "Study of scheduling algorithms for event-based tasks," *GM Internal Research Report*, E3-296, April 1992.
50. J.G. D'Ambrosio, **X. Hu** and B.T. Murray, "A core computer system for quantitative analysis of embedded computer architectures," *GM Internal Research Report*, E3-294, April 1992.
51. **X. Hu**, "Task allocation in a pipeline interleaved event processor," *GM Internal Research Report*, E3-249, April 1991.
52. J.G. D'Ambrosio, **X. Hu**, B.T. Murray, *et al.*, "ECM2000 project proposal," *GM Internal Research Report*, E3-204, July 1990.