Complete Publication List of Xiaobo Sharon Hu

Book Chapters

[B1] Z. Yan*, Q. Lu, Weiwen Jiang, Lei Yang, **X. Hu**, Jingtong Hu and Y. Shi, "Hardware–Software Co-design of Deep Neural Architectures: From FPGAs and ASICs to Computing-in-Memories," *Embedded Machine Learning for Cyber-Physical, IoT, and Edge Computing*, S. Pasricha and M. Shafique (Eds.), Springer, Cham, 2024, pp. 271–301.

[B2] Z. Yan*, **X. Hu** and Y. Shi, "On the Reliability of Computing-in-Memory Accelerators for Deep Neural Networks," *System Dependability and Analytics*, L. Wang, K. Pattabiraman, C. Di Martino, A. Athreya, S. Bagchi (Eds.), Springer, Cham, 2023, pp. 167–190.

[B3] T. Zhang, G. Tao, **X. Hu**, Q. Deng and S. Han, "Dynamic Resource Management in Real-Time Wireless Networks," *Wireless Networks and Industrial IoT*, N.H. Mahmood, N. Marchenko, M. Gidlund, P. Popovski (Eds.), Spinger, 2021, pp. 131–156.

[B4] Y. Ma*, J. Zhou, T. Chantem, R. P. Dick, and **X. Hu**, "Resource Management for Improving Overall Reliability of Multi-Processor Systems-on-Chip," *Dependable Embedded Systems*, J. Henkel and N. Dutt (Eds.), Springer International Publishing, 2021, pp. 233–246.

[B5] Y. Bi, P.-E. Gaillardon, **X. Hu**, M. Niemier, J.-S. Yuan and Y. Jin, "Polarity-Controllable Silicon NanoWire FET-Based Security," *Security Opportunities in Nano Devices and Emerging Technologies*, M. Tehranipoor, D. Forte, G.S. Rose, S. Bhunia (Eds.), Tayor & Francis, 2017, pp. 165–178.

[B6] G. Csaba, G.H. Bernstein, A. Orlov, M.T. Niemier, **X. Hu** and W. Porod, "Nanomagnetic logic: from magnetic ordering to magnetic computing," *CMOS and Beyond: Logic Switches for Terascale Integrated Circuits*, T.-J.K. Liu, K.J. Kuhn (Eds.), Cambridge University Press, 2015, pp. 301–334.

Refereed Journal Articles (published or accepted for publication)

[J1] L. Liu*, M. Sharifi*, K. Wang, R. Mao, K. Ni, C. Li, X. Yin, M. Niemier and **X. Hu**, "EvaCAM: A circuit-level evaluation tool for general content addressable memories," accepted to *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, 2025.

[J2] T. Zhang, J. Wang, **X. Hu** and S Han, "5G-TPS: A two-phase real-time scheduling and adaptation framework for 5G radio access networks," accepted to *IEEE Transactions on Mobile Computing (IEEE TMC)*, 2025.

[J3] Y. Qin*, Z. Yan, W. Wen, **X. Hu** and Y. Shi, "NeFT: Negative Feedback Training to Improve Robustness of Compute-In-Memory DNN Accelerators," accepted to *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, 2025.

*Student or postdoctoral fellow advised or co-advised by X. Sharon Hu at the time of publication.

[J4] A. Mamdouh, H. Geng*, M. Niemier, **X. Hu** and D. Reis, "Shared-PIM: enabling concurrent computation and data flow for faster processing-in-DRAM," accepted to *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, 2025.

[J5] M. Li*, D. Reis, A. F. Laguna, M. Niemier and **X. Hu**, "Accelerating recommendation systems with in-memory embedding operations," accepted to *IEEE Transactions on Circuits and Systems for Artificial Intelligence (IEEE TCAS-AI)*, 2024.

[J6] X. Yin, Q. Huang, H. E. Barkam, F. Müller, S. Deng, A. Vardar, S. De, Z. Jiang, M. Imani, U. Schlichtmann, **X. Hu**, C. Zhuo, T. Kampfe and K. Ni, "A homogeneous FeFET-based time-domain compute-in-memory fabric for matrix-vector multiplication and associative search," accepted to *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, 2024.

[J7] Z. Yan*, **X. Hu** and Y. Shi, "U-SWIM: Universal Selective Write-Verify for computing-in-memory neural accelerators," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 43, No. 6, 2024, pp. 1822–1833.

[J8] F.-X. Liang*, S. Kumar, K. Ni, W. Chakraborty, Y. Chauhan, H. Amrouch, S. Datta, M. T. Niemier and **X. Hu**, "A physics-based model for oxide-semiconductor-based ferroelectric field-effect transistors," *IEEE Transactions on Electronic Devices (IEEE TED)*, Vol. 71, No. 7, 2024, pp. 4397-4402.

[J9] X. Yin, F. Müller, A. F. Laguna, C. Li, Q. Huang, Z. Shi, M. Lederer, N. Laleni, S. Deng, Z. Zhao, M. Imani, Y. Shi, M. Niemier, **X. Hu**, C. Zhuo, T. Kämpfe and K. Ni, "Deep random forest with ferroelectric analog content addressable memory," *Science Advances*, 10(23), 2024, eadk8471.

[J10] Z. Yan*, **X. Hu** and Y. Shi, "Compute-in-memory based neural network accelerators for safety-critical systems: worst-case scenarios and protections," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 43, No. 8, 2024, pp. 2452-2464.

[J11] Y. Xu, Z. Zhao, Y. Xiao, T. Yu, H. Mulaosmanovic, D.Kleimaier, S. Duenkel, S. Beyer,X. Gong, R. Joshi, **X. Hu**, S. Wen, A.S. Rios, K. Lekkala, L. ItItti, E. Homan, S. George,V. Narayanan and K. Ni, "Ferroelectric FET based context-switching FPGA enabling dynamic reconfiguration for adaptive deep learning machines," *Science Advances*, 10(3), 2024, eadk1525.

[J12] X. Yang, Z. Wang, **X. Hu**, C. H. Kim, S. Yu, M. Pajic, R. Manohar, Y. Chen and H. Li, "Neuro-symbolic computing: advancements and challenges in hardware-software co-design", *IEEE Transactions on Circuits and Systems II (TCAS-II)*, Vol. 71, No. 3, 2024, pp. 1683-1689.

[J13] J. Takeshita, D. Reis*, T. Gong, M. T. Niemier, **X. Hu** and T. Jung, "Accelerating Finite-Field and Torus FHE via Compute-Enabled (S)RAM," Special Issue on Near / In-Memory Processing, *IEEE Transactions on Computers (IEEE TC)*, Vol. 73, No. 10, 2024, pp. 2449-2462.

[J14] R. Wang, S. H. Moon, **X. Hu**, X. Jiao and D. Reis, "A computing-in-memory-based one-class hyperdimensional computing model for outlier detection," *IEEE Transactions on Computers (IEEE TC)*, Vol. 73, No. 6, 2024, pp. 1559-1574.

[J15] T. Zhang, T. Gong, M Lyu, N Guan, S Han and **X. Hu**, "Reliable dynamic packet scheduling with slot sharing for real-time wireless networks," *IEEE Transactions on Mobile Computing (IEEE TMC)*, Vol. 22, No. 11, 2023, pp. 6723–6741.

[J16] J. Gong, H. Saadat, H. Gamaarachchi, H. Javaid, **X. Hu** and S. Parameswaran, "ApproxTrain: Fast simulation of approximate multipliers for DNN training and inference," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 42, No. 11, 2023, pp. 3505-3518.

[J17] Z. Zhe, H. Sun, T. Xie, Y. Zhu, G. Dai, L. Xia, D. Niu, X. Chen,, **X. Hu** , Y. Cao, Y. Xie, H. Yang and Y. Wang, "MNSIM 2.0: A behavior-level modeling tool for processing-in-memory architectures," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 42, No. 11, 2023, pp. 4112–4125.

[J18] Z. Jia, J. Chen, X. Xu, J. Kheir, J. Hu, H. Xiao, S. Peng, **X. Hu**, D. Chen and Y. Shi, "The importance of resource awareness in artificial intelligence for healthcare," *Nature Machine Intelligence*, 2023, pp. 1–12.

[J19] R. Zhang, C. Tang, X. Sun, M. Li*, W.Jin, P. Li, X. Cheng and **X. Hu**, "Sky-TCAM: Low-power skyrmion-based ternary content addressable memory," *IEEE Transactions on Electronic Devices (IEEE TED)*, Vol. 70, No. 7, 2023, pp. 3517–3522.

[J20] B. Wu, D. Reis, Z. Wang, Y. Wang, K. Chen, W. Liu, F. Lombardi and **X. Hu** , "An energy-efficient computing-in-memory (CiM) scheme using field-free spin orbit torque (SOT) magnetic RAMs," *IEEE Transactions on Emerging Topics in Computing (IEEE TETC)*, Vol. 11, No. 2, 2023, pp. 331–342.

[J21] G. Cauwenberghs, J. Cong, **X. Hu**[+], S. Joshi, S. Mitra, W. Porod and H.-S. P. Wong, "Micro/nano circuits and systems design and design automation: challenges and opportunities" *Proceedings of the IEEE*, Vol. 111, No. 6, 2023, pp. 561–574.

[J22] M. Yang, Q. Lou, R. Rajaei, M. R. Jokar, J. Qiu, Y. Liu, A. Udupa, F. T. Chong, J. M. Dallesasse, M. Feng, L. L. Goddard, **X. Hu** and Y. Li, "A hybrid optical-electrical analog deep learning accelerator using incoherent optical signals," *ACM Journal on Emerging Technologies in Computing Systems (ACM JETC)*, Vol. 19, No. 2, Article 14, 2023, pp. 1–24.

[J23] L. Liu*, A.F. Laguna, R. Rajaei, M.M. Sharifi*, A. Kazemi, X. Yin, M. Niemier and **X. Hu**, "A reconfigurable FeFET content addressable memory For multi-state Hamming distance," *IEEE Transactions on Circuits and Systems I (IEEE TCAS I)*, Vol. 70, No. 6, 2023, pp. 2356–2369.

[J24] S. Narla, P. Kumar, A. F. Laguna, D. Reis, **X. Hu**, M. Niemier and A. Naeemi, "Design of a compact spin-orbit-torque based ternary content addressable memory," *IEEE Transactions on Electronic Devices (IEEE TED)*, Vol. 70, No. 2, 2023, pp. 506–513.

[+]Corresponding author.

[J25] M. Li*, P. Wu, B. Zhou, J. Appenzeller and **X. Hu**, "Cross-coupled Gated tunneling diodes with unprecedented PVCRs enabling compact SRAM design—Part II: SRAM circuit," *IEEE Transactions on Electron Devices (IEEE TED)*, Vol. 69, No. 11, 2022, pp. 6085–6088.

[J26] P. Wu, M. Li*, B. Zhou, **X. Hu** and J. Appenzeller, "Cross-coupled Gated tunneling diodes with unprecedented PVCRs enabling compact SRAM design—Part I: Device concept," *IEEE Transactions on Electron Devices (IEEE TED)*, Vol. 69, No. 11, 2022, pp. 6078–6084.

[J27] R. Mao, B. Wen, A. Kazemi*, Y.Zhao, A. F. Laguna*, R.Lin, N. Wong, M. Niemier, **X. Hu**, X. Sheng, C. E. Graves, J. P. Strachan and C. Li, "Experimentally validated memristive memory augmented neural network with efficient hashing and similarity search," *Nature Communications*, Vol. 13, No. 1, 2022, pp. 1–13.

[J28] A. Kazemi*, F. Müller, M. M. Sharifi*, H. Errahmouni, G. Gerlach, T. Kämpfe, M. Imani, **X. Hu** and M. Niemier, "Achieving software-equivalent accuracy for hyperdimensional computing with ferroelectric-based in-memory computing," *Scientific Reports*, Vol. 12, 2022, Article No.: 19201.

[J29] S. Narla, P. Kumar, D. Reis∗, A. F. Laguna∗, M. Niemier, **X. Hu** and A. Naeemi, "Modeling and design for magnetoelectric ternary content addressable memory (TCAM)," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (IEEE JxCDC)*, Vol. 8, No. 1, 2022, pp. 44–52.

[J30] T. Wang, J. Zhou, L. Li, G. Zhang, K. Li and **X. Hu**, "Deadline and reliability aware multi-server configuration optimization for maximizing profit," *IEEE Transactions on Parallel and Distributed Systems (IEEE TPDS)*, Vol. 33, No. 12, 2022, pp. 3772–3786.

[J31] A. F. Laguna*, M.M. Sharifi*, A. Kazemi*, X. Yin*, M. Niemier and **X. Hu**, "Hardware-software co-design of an in-memory transformer network accelerator," *Frontiers in Electronics, Section Integrated Circuits and VLSI*, 2022, 3:847069.

[J32] S. Mishra*, D.Z. Chen and **X. Hu**, "Data-driven Deep supervision for medical image segmentation," *IEEE Transactions on Medical Imaging (IEEE TMI)*, Vol. 41, No. 6, 2022, pp. 1560–1574.

[J33] A. Kazemi*, M. M. Sharifi*, A. F. Laguna*, F. Müller, X. Yin, T. Kämpfe, M. Niemier and **X. Hu**, "FeFET multi-bit content-addressable memories for in-memory nearest neighbor search," *IEEE Transactions on Computers (IEEE TC)*, Vol. 71, No. 10, 2022, pp. 2565–2576.

[J34] D. Reis*, M. Niemier and **X. Hu**, ""IMCRYPTO: An in-memory computing fabric for AES encryption and decryption," *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 30, No. 5, 2022, pp. 553–565.

[J35] Q. Huang, D. Reis*, C. Li, D. Gao, M. T. Niemier, **X. Hu**, M. Imani, X. Yin and C. Zhuo, "Computing-in-emory using ferroelectrics: from single- to multi-input logic," Special Issue on Near-Memory and In-Memory Processing, *IEEE Design & Test of Computers*, Vol. 39, No. 2, 2022, pp. 56–64.

[J36] L. Zhang, S. Mishra*, T. Zhang*, Y. Zhang, D. Zhang, Y. Lv, M. Lv, N. Guan, **X. Hu**, D. Z. Chen and X. Han, "Design and assessment of convolutional neural network based methods for vitiligo diagnosis," *Frontiers in Medicine, section Dermatology*, 2021, 8:754202.

[J37] S. Mishra*, D. Z. Chen and **X. Hu**, "Image complexity guided network compression for biomedical image segmentation," *ACM Journal on Emerging Technologies in Computing Systems (ACM JETC)*, Vol. 18, No. 2, Article 26, 2021, pp. 1–23.

[J38] S. Mishra*, Y. Wang, C. Wei, D. Z. Chen and **X. Hu**, "VTG-Net: A CNN based vessel topology graph network for retinal artery/vein classification," *Frontiers in Medicine*, Vol. 8, 2021, pp. 2124 (10 pages).

[J39] D. Reis*, M. T. Niemier and **X. Hu**, "The implications of ferroelectric FET device models to the design of computing-in-memory architectures," Special Issue on Future Trends in Nanocomputing, *Journal of Integrated Circuits and Systems*, Vol. 16, No. 1, 2021, pp. 1–8.

[J40] T. Zhang*, T. Gong, S. Han, Q. Deng and **X. Hu**, "Fully distributed packet scheduling framework for handling disturbances in lossy real-time wireless networks," *IEEE Transactions on Mobile Computing (IEEE TMC)*, Vol. 20, No. 2, 2021, pp. 502–518.

[J41] B. Wu*, Z. Wang, Y. Li, Y. Wang, D. Liu, W. Zhao and **X. Hu**, "A NAND-SPIN based magnetic ADC," *IEEE Transactions on Circuits and Systems II: Express Briefs (IEEE TCAS II)*, Vol. 68, No. 2, 2021, pp. 617–621.

[J42] X. Xu, X. Zhang, B. Yu, **X. Hu**, C. Rowen, J. Hu and Y. Shi, "DAC-SDC low power object detection challenge for UAV applications," *IEEE Transactions on Pattern Analysis and Machine Intelligence (IEEE PAMI)*, Vol. 43, No. 2, 2021, pp. 392–403.

[J43] R. Rajaei*, M. M. Sharifi*, A. Kazemi*, M. Niemier and **X. Hu**, "Compact single-phase-search multi-state content addressable memory design using 1 FeFET/cell," *IEEE Transactions on Electron Devices (IEEE TED)*, Vol. 68, No. 1, 2021, pp. 109–117.

[J44] Y. Xi, H. Wu, B. Gao, J. Tang, A. Chen, M.-F. Chang, **X. Hu**, J. Van der Spiegel and H. Qian, "In-memory learning with analog resistive switching memory: a review and perspective," *Proceedings of the IEEE*, Vol. 109, No. 1, 2021, pp. 14–42.

[J45] P. Wu, D. Reis*, **X. Hu** and J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics*, Vol. 4, 2021, pp. 45–53.

[J46] L. Li, J. Zhou*, M. Chen, T. Wei and **X. Hu**, "Learning-based modeling and optimization for real-time system availability," Special Issue on Machine-Learning Architectures and Accelerators, *IEEE Transactions on Computers (IEEE TC)*, Vol. 70, No. 4, 2020, pp. 581–594.

[J47] W. Jiang, Q. Lou*, Z. Yan*, L.Yang, J. Hu, **X. Hu** and Y. Shi "Device-circuit-architecture co-exploration for computing-in-memory neural accelerators," *IEEE Transactions on Computers (IEEE TC)*, Vol. 70, No. 4, 2020, pp. 595–605.

[J48] D. Gao, D. Reis*, **X. Hu** and C. Zhuo, "Eva-CiM: a system-level performance and energy evaluation framework for computing-in-memory architectures," *IEEE Transactions*

on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD), Vol. 39, No. 12, pp. 5011–5024, 2020.

[J49] Y. Ding, W. Jiang, Q. Lou*, J. Liu, J. Xiong, **X. Hu**, X. Xu, and Y. Shi, "Hardware design and the competency awareness of a neural network," *Nature Electronics*, Vol. 3, 2020, pp. 514–523.

[J50] F. Molnàr, S.R. Kharel, **X. Hu** and Z. Toroczkai, "Accelerating a continuous-time analog SAT solver using GPUs," *Computer Physics Communications*, Vol. 256, 2020, 107469.

[J51] D.Y. Zhang, Y. Ma*, **X. Hu** and D. Wang, "Towards privacy-aware task allocation in social sensing based edge computing systems," *IEEE Internet of Things Journal (IEEE IoT-J)*, Vol. 7, No. 12, 2020, pp. 11384–11400.

[J52] B. Wu*, C. Wang, Z. Wang, Y. Wang, D. Zhang, D. Liu, Y. Zhang and **X. Hu**, "Field-free 3T2SOT MRAM for non-volatile cache memories," *IEEE Transactions on Circuits and Systems I (IEEE TCAS I)*, Vol. 67, No. 12, 2020, pp. 4660–4669.

[J53] D. Reis*, J. Takeshita, T. Jung, M. Niemier and **X. Hu**, "Computing-in-Memory for performance and energy efficient homomorphic encryption," *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 28, No. 11, 2020, pp. 2300–2313.

[J54] H. Wang , N. C. Audsley , **X. Hu** and W. Chang, "Meshed Bluetree: Time-predictable multi-memory interconnect for multi-core architectures," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 39, No. 11, 2020, pp. 3787-3798.

[J55] Y. Ma*, J. Zhou*, T. Chantem*, R. Dick, S. Wang and **X. Hu**, "Improving reliability of real-time embedded systems on integrated CPU and GPU platforms," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 39, No. 10, 2020, pp. 2218-2229.

[J56] M. Imani, X. Yin*, J, Messerly, S. Gupta, M. Nemier, **X. Hu** and T. Rosing, "SearcHD: A memory-centric hyperdimensional computing with stochastic training," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 39, No. 10, 2020, pp. 2422-2433.

[J57] C. Leng, Y. Qiao, **X. Hu** and H. Wang, "Co-Scheduling aperiodic real-time tasks with end-to-end firm and soft deadlines in two-stage systems," *Real-Time Systems (RTS)*, Vol. 56, 2020, pp. 56, 391–451.

[J58] Y. Ding, W. Jiang, Q. Lou*, J. Liu, J. Xiong, **X. Hu**, X. Xu, and Y. Shi, "Hardware design and the competency awareness of a neural network," *Nature Electronics*, Vol. 3, 2020, pp. 514–523.

[J59] B. Wu*, P. Dai, Z. Wang, C. Wang, Y. Wang, J. Yang, Y. Cheng, D. Liu, Y. Zhang, W. Zhao and **X. Hu**, "Bulkyflip: A NAND-SPIN based last-level cache with bandwidth-oriented write management policy," *IEEE Transactions on Circuits and Systems I: Regular Papers (IEEE TCAS I)*, Vol. 67, No. 1, 2020, pp. 108–120.

[J60] X. Chen*, S. Datta, **X. Hu**, M. Jerry, A.Laguna*, K. Ni, M. Niemier, D. Reis*, X. Sun, P. Wang, X.Yin* and S. Yu, "The impact of ferroelectric FETs on digital and analog circuits and architectures," *IEEE Design & Test*, Vol. 37, No. 1, 2020, pp. 79–99.

[J61] X. Yin*, C. Li, Q. Huang, L. Zhang, M. Niemier, **X. Hu**, C. Zhuo and K. Ni, "FeCAM: A universal compact digital and analog content addressable memory using ferroelectric," *IEEE Transactions on Electron Devices (IEEE TED)*, Vo. 67, No. 7, 2020, pp. 2785-2792.

[J62] J. Chen, H. Wu, B. Gao, J. Tang, **X. Hu** and H. Qian, "A parallel multi-bit programming scheme with high precision for RRAM-based neuromorphic systems," *IEEE Transactions on Electron Devices (IEEE TED)*, Vol. 67, No. 5, 2020, pp. 2213–2217.

[J63] Y.Ma*, J. Zhou, T. Chantem*, R. Dick, S. Wang and **X. Hu**, "On-line resource management for improving reliability of real-time systems on "Big–Little" type MPSoCs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 39, No. 1,2020, pp. 88–100.

[J64] T. Zhang*, T. Gong, S. Han, Q. Deng and **X. Hu**, "Distributed dynamic packet scheduling framework for handling disturbances in real-time wireless networks," *IEEE Transactions on Mobile Computing (IEEE TMC)*, Vol. 18, No. 11, 2019, pp. 2502–2517.

[J65] C. Pan, Q. Lou*, M. Niemier, **X. Hu** and A. Naeemi, "Energy-efficient convolutional neural network based on cellular neural network using beyond-CMOS technologies," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (IEEE JxCDC)*, Vol. 5, No. 2, 2019, pp. 85–93.

[J66] J. Zhou*, X. Zhou, J. Sun, T. Wei, M. Chen, S. Hu and **X. Hu**, "Resource management for improving soft-error and lifetime reliability of real-time MPSoCs" *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 38, No. 12, 2019, pp. 2215–2228.

[J67] D. Reis*, M. Niemier and **X. Hu**, "A computing-in-memory engine for searching on homomorphically encrypted data," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (IEEE JxCDC)*, Vol. 5, No. 2, 2019, pp. 123–131.

[J68] D. Reis*, K. Ni, W. Chakraborty, X. Yin*, M. Trentzsch, S. Dünkel, J. Müller, S. Beyer, S. Datta, M. Niemier and **X. Hu**, "Design and analysis of an ultra-dense, low-leakage and fast FeFET-based random access memory array," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (IEEE JxCDC)*, Vol. 5, No. 2, 2019, pp. 103–112.

[J69] A. Stephan, Q. Lou*, M. Niemier, **X. Hu** and S. Koester, "Nonvolatile spintronic memory cells for neural networks," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (IEEE JxCDC)*, Vol. 5, No. 2, 2019, pp. 67–73.

[J70] K. Ni, X. Yin*, A. Laguna*, S. Joshi, S. Dünkel, M. Trentzsch, J. Müeller, S. Beyer, W. Taylor, M. Niemier, **X. Hu** and S. Datta, "Ferroelectric ternary content addressable memory for one-shot learning," *Nature Electronics*, Vol. 2, No. 11, 2019, pp 521–529.

[J71] A. Chen, S. Datta, **X. Hu**, M. Niemier, T. Simunic Rosing and J. J. Yang, "A survey on architecture advances enabled by emerging beyond-CMOS technologies," *IEEE Design & Test*, Vol. 36, No. 3, 2019, pp. 46–68.

[J72] J. Zhou*, **X. Hu**, Y. Ma*, J. Sun, T. Wei and S. Hu, "Improving availability of multicore real-time systems suffering both permanent and transient faults," *IEEE Transactions on Computers (IEEE TC)*, Vol.68, No. 12, 2019, pp. 1785–1801.

[J73] Q. Lou*, C. Pan, J. Mcguinness, A. Horvath, A. Naeemi, M Niemier and **X. Hu**, "A mixed signal architecture for convolutional neural networks," *ACM Journal on Emerging Technologies in Computing Systems (ACM JETC)*, Vo. 15, No. 2, 2019, Article No. 19.

[J74] X. Yin*, K. Ni, D. Reis, S. Datta, M. Niemier and **X. Hu**, "An ultra-dense 2FeFET TCAM design based on a multi-domain FeFET model," *IEEE Transactions on Circuits and Systems II: Express Briefs (IEEE TCAS II)*, Vol. 66, No. 9, 2019, pp. 1577–1581.

[J75] X. Chen*, D. Chen, Y. Han and **X. Hu**, "moDNN: Memory optimal deep neural network training on Graphics Processing Units," *IEEE Transactions on Parallel and Distributed Systems (IEEE TPDS)*, Vol. 30, No. 3, 2019, pp. 646–661.

[J76] X. Yin*, X. Chen*, M. Niemier and **X. Hu**, "Ferroelectric FETs based nonvolatile logic-in-memory circuits," *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 27, No. 1, 2019, pp. 159–172.

[J77] L. Li, P. Cong, K. Cao, J. Zhou*, T. Wei, M. Chen, S. Hu and **X. Hu**, "Game theoretic feedback control for reliability enhancement of EtherCAT-based networked systems," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 38, No. 9, 2019, pp. 1599–1610.

[J78] K. Cao, J. Zhou*, T. Wei, M. Chen, S. Hu and **X. Hu**, "Affinity-driven modeling and task scheduling for makespan optimization in heterogeneous multiprocessor systems considering reliability and temperature," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 38, No. 7, 2019, pp. 1189–1202.

[J79] X. Chen*, K. Ni, M. Niemier, Y. Han, S. Datta and **X. Hu**, "Power and area efficient FPGA building blocks based on ferroelectric FETs," *IEEE Transactions on Circuits and Systems I: Regular Papers (IEEE TCAS I)*, Vol. 66, No. 5, 2019, pp. 1780–1793.

[J80] **X. Hu** and M. Niemier, "Cross-layer efforts for energy-efficient computing—Towards peta operations per second per watt," *Frontiers of Information Technology & Electronic Engineering*, Vol. 19, No. 10, 2018, pp. 1209–1223.

[J81] M. Jerry, S. Dutta, A. Kazemi, K. Ni, J. Zhang, P.-Y. Chen, P. Sharma, S. Yu, **X. Hu**, M. Niemier and S. Datta, "A ferroelectric field effect transistor based synaptic weight cell," *Journal of Physics D: Applied Physics*, Vol. 51, No. 43, 2018, pp. 434001.

[J82] R. Perricone*,**X. Hu**, J. Nahas, and M. Niemier, "Can beyond CMOS devices illuminate dark silicon," *Communications of the ACM (CACM) (ACM CACM)*, Vol. 61, No. 9, 2018, pp. 60–69.

[J83] T. Wei, J. Zhou, K. Cao, P. Cong, M. Chen, G. Zhang, **X. Hu** and J. Yan, "Cost-constrained QoS optimization for approximate computation real-time tasks in heterogeneous MPSoCs," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 37, No. 9, 2018, pp. 1733–1746.

[J84] X. Yin*, B. Sedighi, M. Varga, M. Ercsey-Ravasz, Z. Toroczkai and **X. Hu**, "Efficient analog circuits for Boolean satisfiability," *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 26, No. 1, 2018, pp. 155–167.

[J85] X. Xu, Y. Ding, **X. Hu**, M. Niemier, J. Cong, Y. Hu and Y. Shi, "Scaling for edge inference of deep neural networks," *Nature Electronics*, Vol. 1, No. 4, 2018, pp. 216–222.

[J86] T. Wu, Y. Liu, D. Zhang, J. Li, **X. Hu**, C. J. Xue and H. Yang. "DVFS based long-term task scheduling for dual-channel solar-powered sensor nodes," *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 25, No. 11, 2017, pp. 2981–2994.

[J87] Y. Ma*, T. Chantem*, R.P. Dick and **X. Hu**, "Improving system-level lifetime reliability of multicore soft real-time systems," *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 25, No. 6, 2017, pp. 1895–1905.

[J88] Y. Bi, K. Shamsi, J. Yuan, Y. Jin, M.T. Niemier and **X. Hu**, "Tunnel FET current mode logic for DPA resilient circuit designs," *IEEE Transactions on Emerging Topics in Computing (IEEE TETC)*, Vol. 5, No. 3, 2017, pp. 340–352.

[J89] L. Tang*, **X. Hu**, R. Barrett and J Cook, "PeaPaw: Performance and energy aware partitioning of workload on heterogeneous platforms," *ACM Transactions on Design Automation of Electronic Systems (ACM TODAES)*, Vol. 22, No. 3, 2017, pp. 41:1–41:26.

[J90] J. Fernandez-Berni, M. Niemier, **X. Hu**, H. Lu, W. Li, P. Fay, R. Carmona-Galan and A. Rodriguez-Vazquez, "TFET-based well capacity adjustment in active pixel sensor for enhanced high dynamic range," *Electronic Letters*, Vol. 53, No. 9, 2017, pp. 622–624.

[J91] T. Liu, H. Guo, S. Parameswaran and **X. Hu**, "iCETD: An improved tag generation design for memory data authentication in embedded processor systems," *Integration, the VLSI Journal*, Vol. 56, pp. 96–104, 2017.

[J92] Y. Bi, K. Shamsi, P.E. Gaillardon, G.de Micheli, X. Yin*, **X. Hu**, M.T. Niemier, J. Yuan and Y. Jin, "Emerging technology based design of primitives for hardware security," *ACM Journal on Emerging Technologies in Computing (ACM JETC)*, Vo. 13, No. 1, 2016, pp. 3:1–3:19.

[J93] J. Zhou*, T. Wei, M. Chen, J. Yan, **X. Hu** and Y. Ma*, "Thermal-aware task scheduling for energy minimization in heterogeneous real-time MPSoC systems," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 35, No. 8, 2016, pp. 1269–1282.

[J94] D. Zhang, S. Li, Y. Liu, **X. Hu**, X. He, Y. Zhang, P. Zhang and H. Yang, "A C2RTL framework supporting partition, parallelization, and FIFO sizing for streaming applications," *ACM Transactions on Design Automation of Electronic Systems (ACM TODAES)*, Vol. 21, No. 2, 2016, pp. 19:1–19:32.

[J95] R. Perricone*, Y. Liu*, A. Dingler*, **X. Hu** and Michael Niemier, "Design of stochastic computing circuits using nanomagnetic logic," *IEEE Transactions on Nanotechnology (IEEE TNANO)*, Vol. 15, No. 2, 2016, pp. 179–187.

[J96] K. Xiao*, **X. Hu**, B. Zhou* and D.Z. Chen, "Shell: A spatial decomposition data structure for ray traversal on GPU," *IEEE Transactions on Computers (IEEE TC)*, Vol. 65, No. 1, 2016, pp. 230–243.

[J97] S. Hong*, T. Chantem* and **X. Hu**, "Local-deadline assignment for distributed real-time systems," *IEEE Transactions on Computers (IEEE TC)*, Vol. 64, No. 7, 2015, pp. 1983–1997.

[J98] F.A. Shah, G. Csaba, M.T. Niemier, **X. Hu**, W. Porod and G. Bernstein, "Error analysis for ultra dense nanomagnet logic circuits," *Journal of Applied Physics (JAP)*, Vol. 117, No. 17, 2015, 17A906.

[J99] C. Leng, Y. Qiao, **X. Hu** and H. Wang, "Utilization-based admission control for aperiodic tasks under EDF scheduling," *Real-Time Systems*, Vol. 51, No. 1, 2015, pp. 36–76.

[J100] B. Sedighi*, **X. Hu**, H. Liu, J.J. Nahas and M.T. Niemier, "Analog circuit design using tunnel-FETs," *IEEE Transactions on Circuits and Systems I (IEEE TCAS I)*, Vol. 62, No. 1, 2015, pp. 39–48.

Refereed Conference Papers (published or accepted for publication)

[C1] K. Wu, T. Zhang, **X. Hu** and S. Han, "Flexibility-aware network resource partitioning for multi-state real-time mission-critical applications," *IEEE real-time symposium (RTSS)* (IEEE), December 2025.

[C2] H. Geng*, X. Lu, Y. Che, Z. Tian, D. Cheng, X. Sun, M. Niemier and **X. Hu**, "COSMOS: RL-enhanced locality-aware counter cache optimization for secure memory," *International Symposium on Microarchitecture (MICRO)* (IEEE/ACM). October 2025.

[C3] R. Qin, P. Ren*, Z. Yan, L. Liu*, D. Liu, A. Nassereldine, J. Xiong, K. Ni, **X. Hu** and Y. Shi, "NVCiM-PT: An NVCiM-assisted prompt tuning framework for edge LLMs," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), April 2025.

[C4] Y Qin*, Z. Jia, Z. Yan, J. Mok, M. Yung, Y. Liu, X. Liu, W. Wen, L. Liang, K.T. Cheng, **X. Hu** and Y. Shi, "A 10.60 uW 150 GOPS mixed-bit-width sparse CNN accelerator for life-threatening ventricular arrhythmia detection," *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2025.

[C5] C. Ni, S. Chen, L. Liu*, M. Imani, T. Kämpfe, K. Ni, M. Niemier, **X. Hu**, C. Zhuo and X. Yin, "TAP-CAM: A tunable approximate matching engine based on ferroelectric content addressable memory," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), October 2024.

[C6] L. Pei, Y. Qin*, Z.M. Enciso, B. Cheng, J. Liu, S. Davis, Z. Jia, M. Niemier, Y. Shi, **X. Hu** and N. Cao, "Towards uncertainty-quantifiable biomedical intelligence: mixed-signal compute-in-entropy for Bayesian neural networks," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), October 2024.(Nominated for the **Best Paper** Award.)

[C7] Y Qin*, Z. Yan, Z. Pan, W. Wen, **X. Hu** and Y. Shi, "TSB: Tiny shared block for efficient DNN deployment on NVCIM accelerators," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), October 2024.

[C8] H. Farzaneh, J. P. Cardoso De Lima, M Li*, A. A. Khan, **X. Hu** and J. Castrillon, "C4CAM: A Compiler for CAM-based In-memory Accelerators," *ACM International Conference on Architectural Support for Programming Languages and Operating System (ASPLOS)* (ACM), April 2024, Volume 3.

[C9] T. Zhang, J. Wang, **X. Hu** and S. Han, "Real-time flow scheduling in industrial 5G new radio," *IEEE real-time symposium (RTSS)* (IEEE), December 2023, pp. 371–384.

[C10] J. Wang, T. Zhang, Q. Deng, **X. Hu** and S. Han, "Resource virtualization with end-to-end timing guarantees for multi-hop multi-channel real-time wireless networks," *IEEE real-time symposium (RTSS)* (IEEE), December 2023, pp. 385–396.

[C11] M Li*, H. Geng*, M. Niemier and **X. Hu**, "Accelerating polynomial modular multiplication with crossbar-based compute-in-memory," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2023, pp. 1–9.

[C12] Z. Yan*, Y. Qin, W. Wen, **X. Hu** and Y. Shi, "Improving realistic worst-case performance of NVCiM DNN accelerators through training with right-censored Gaussian noise," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2023, pp. 1-9. (Received the **William J. McCalla ICCAD Best Paper** Award.)

[C13] S. Shou, C. Liu, S. Yun, Z. Wan, K. Ni, M. Imani, **X. Hu**, J. Yang, C. Zhuo and X. Yin, "SEE-MCAM: Scalable multi-bit FeFET content addressable memories for energy efficient associative search," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2023, pp. 1-9.

[C14] L. Liu*, S. Kumar, S. Thomann, H. Amrouch and **X. Hu**, "Compact and high-performance TCAM based on scaled double-gate FeFETs," *Design Automation Conference (DAC)* (ACM/IEEE), July 2023, pp. 1-6.

[C15] T. Zhang*, **X. Hu** and S. Han, "Contention-free configured grant scheduling for 5G URLLC traffics," *Design Automation Conference (DAC)* (ACM/IEEE), July 2023, pp. 1-6.

[C16] M. Li*, A. Kazemi*, A. F. Laguna* and **X. Hu**, "Associative memory based experience replay for deep reinforcement learning," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2022. Article No. 135, pp. 1–9.

[C17] C.-K. Liu, H. Chen, M. Imani, K. Ni, A. Kazemi*, A. F. Laguna*, M. Niemier, **X. Hu**, L. Zhao, C. Zhuo and X. Yin, "COSIME: FeFET based associative memory for in-memory cosine similarity search," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2022. Article No. 137, pp. 1–9.

[C18] Z. Yan*, **X. Hu** and Y. Shi, "Computing-in-memory neural network accelerators for safety-critical systems: Can small device variations be disastrous?" *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2022. Article No. 87, pp. 1–9.

[C19] S. Mishra*, Y. Zhang, L. Zhang, T. Zhang, **X. Hu** and D. Z. Chen, "Data-driven deep supervision for skin lesion classification," *International Conference on Medical Image Computing and Computer-Assisted Intervention (MICCAI)*, September 2022, pp. 721–731.

[C20] D. Shen*, T. Zhang*, J. Wang, Q. Deng, S. Han and **X. Hu**, "QoS guaranteed resource allocation for coexisting eMBB and URLLC traffic in 5G industrial networks," *IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA)* (IEEE), August 2022, pp. 81-90.

[C21] D. Shen*, T. Zhang*, J. Wang, Q. Deng, S. Han and **X. Hu**, "Distributed successive packet scheduling for multi-channel real-time wireless networks," *IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA)* (IEEE), August 2022, pp. 71-80.

[C22] J. Wang, T. Zhang*, D. Shen*, **X. Hu** and S. Han, "HARP: Hierarchical resource partitioning in dynamic industrial wireless networks," *IEEE International Conference on Distributed Computing Systems (ICDCS)* (IEEE), July 2022, pp. 1029–1039.

[C23] R. Wang, X. Jiao and **X. Hu**, "ODHD: One-class hyperdimensional computing for outlier detection," *Design Automation Conference (DAC)* (ACM/IEEE), July 2022, pp. 43-48.

[C24] Z. Yan*, **X. Hu** and Y. Shi, "SWIM: Selective write-verify for computing-in-memory neural accelerators," *Design Automation Conference (DAC)* (ACM/IEEE), July 2022, pp. 277–282.

[C25] M. Li*, A.F. Laguna*. D. Reis*, X. Yin*, M. Niemier and **X. Hu**, "iMARS: An in-memory-computing architecture for recommendation systems," *Design Automation Conference (DAC)* (ACM/IEEE), July 2022, pp. 463–468.

[C26] M. Chang, X. Yin*, Z. Toroczkai, **X. Hu** and A. Raychowdhury, "An analog clock-free compute fabric based on continuous-time dynamical system for solving combinatorial optimization problems," *IEEE Custom Integrated Circuits Conference (CICC)* (IEEE), April 2022, pp. 1–2.

[C27] N. Bagga, K. Ni, N. Chauhan, O. Prakash, **X. Hu** and H. Amrouch, "Cleaved-gate ferroelectric FET for reliable multi-level cell storage," *IEEE International Reliability Physics Symposium (IRPS)* (IEEE), March 2022, pp. P5-1–P5-5.

[C28] L. Liu*, M. M. Sharifi*, R. Rajaei*, A. Kazemi*, K. Ni, X. Yin*, M. Niemier and **X. Hu**, "Eva-CAM: A circuit/architecture-level evaluation tool for general content addressable memories," *Design, Automation & Test in Europe Conference & Exhibition (DATE)* (ACM/IEEE), 2022, pp. 1173–1176.

[C29] Z. Yan*, W. Jiang, **X. Hu** and Y. Shi, "RADARS: Memory efficient reinforcement learning aided differentiable neural architecture search," *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2022, pp. 128–133.

[C30] S. Dutta, A. Khanna, H. Ye, M.M. Sharifi*, A. Kazemi*, M.San Jose, K.A. Aabrar, J.G. Mir, M. Niemier, **X. Hu** and S. Datta, "Lifelong learning with monolithic 3D ferroelectric ternary content-addressable memory," *IEEE International Electron Devices Meeting (IEDM)* (IEEE), 2021, pp. 17.1.1–17.1.4.

[C31] R. Rajaei*, M. Niemier and **X. Hu**, "Low-cost sequential logic circuit design considering single event double-node upsets and single event transients," *IEEE International Conference on Computer Design (ICCD)*, (IEEE), September 2021, pp. 178–185.

[C32] A. Kazemi*, S. Sahay, A. Saxena, M. M. Sharifi*, M. Niemier and **X. Hu**, "A flash-based multi-bit content-addressable memory with Euclidean squared distance," *International Symposium on Low Power Electronics and Design (ISLPED)* (IEEE/ACM), July 2021, 6 pages.

[C33] A. Kazemi*, M. M. Sharifi*, Z. Zou, M. Niemier, **X. Hu** and M. Imani, "MIMHD: Accurate and efficient hyperdimensional inference using multi-bit In-memory computing," *International Symposium on Low Power Electronics and Design (ISLPED)* (IEEE/ACM), July 2021, 6 pages.

[C34] M. M. Sharifi*, L. Pentecost, R. Rajaei*, A. Kazemi*, Q. Lou*, G-Y. Wei, D. Brooks, K. Ni, **X. Hu**, M. Niemier and M. Donato, "Application-driven design exploration for dense ferroelectric embedded non-volatile memories," *International Symposium on Low Power Electronics and Design (ISLPED)* (IEEE/ACM), July 2021, 6 pages.

[C35] M. Yang, M. R. Jokar, J. Qiu, Q. Lou*, Y. Liu, A. Udupa, F. T. Chong, J. M. Dallesasse, M. Feng, L. L. Goddard, **X. Hu** and Y. Li, "A hybrid optical-electrical analog deep learning accelerator using incoherent optical signals," *Great Lakes Symposium on VLSI (GLSVLSI)* (ACM), June 2021, pp. 271–276.

[C36] J. Wang, T. Zhang*, D. Shen*, **X. Hu** and S. Han, "APaS: An adaptive partition-based scheduling framework for 6TiSCH networks," *IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)* (IEEE), May 2021, pp. 320–332.

[C37] S. Thomann, C. Li, C. Zhuo, O. Prakash, X. Yin*, **X. Hu** and H. Amrouch, "On the reliability of in-memory computing: impact of temperature on ferroelectric TCAM," *IEEE VLSI Test Symposium (VTS)* (IEEE), April 2021, pp. 1–6. (Nominated for the **Best Paper** Award.)

[C38] S. Mishra*, D. Chen and **X. Hu**, "Objective-dependent uncertainty driven retinal vessel segmentation," *IEEE International Symposium on Biomedical Imaging (ISBI)* (IEEE), April 2021, pp. 453–457.

[C39] M. Li* and **X. Hu**, "A quantization framework for neural network adaption at the edge," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), 2021, pp. 402–407.

[C40] A. Kazemi*, M.M. Sharifi*, A.F. Laguna*, F. Mueller, R. Rajaei*, R. Olivo, T. Kaempfe, M. Niemier and **X. Hu**, "In-memory nearest neighbor search with FeFET multi-bit content-addressable memories," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), 2021, pp. 1084–1089. (Nominated for the **Best Paper** Award.)

[C41] A.F. Laguna*, A. Kazemi*, M. Niemier and **X. Hu**, "In-memory computing based accelerator for transformer networks for long sequences," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), 2021, pp. 1839–1844.

[C42] D. Reis*, A.F. Laguna*, M. Niemier and **X. Hu**, "Attention-in-memory for few-shot learning with configurable ferroelectric FET arrays," *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2021, pp. 49–54.

[C43] J. S.Takeshita, D. Reis*, T. Gong, M. Niemier, **X. Hu** and T. Jung, "Algorithmic acceleration of B/FV-like somewhat homomorphic encryption for compute-enabled RAM," *Selected Areas in Cryptography*, 2020.

[C44] A.F. Laguna*, H. Gamaarachchi, X. Yin*, M. Niemier, S. Parameswaran and **X. Hu**, "Seed-and-vote based in-memory accelerator for DNA read mapping," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2020. Article No. 56, pp. 1–9.

[C45] X. Dai, S. Zhao, Y. Jiang, X. Jiao, **X. Hu** and W. Chang, "Fixed-priority scheduling and controller co-design for time-sensitive networks," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2020. Article No. 99, pp. 1–9.

[C46] A. Kazemi*, R. Rajaei*, K. Ni, S. Datta, M. Niemier and **X. Hu**, "A hybrid FeMFET-CMOS analog synapse circuit for neural network training and inference," *International Symposium on Circuits and Systems (ISCAS)* (IEEE), October 2020, pp. 1–5.

[C47] R. Rajaei*, Y.-K. Lin, S. Salahuddin, M. Niemier and **X. Hu**, "Dynamic memory and sequential logic design using negative capacitance FinFETs," *International Symposium on Circuits and Systems (ISCAS)* (IEEE), October 2020, pp 1–5.

[C48] R. Rajaei*, Y.K. Lin, S. Salahuddin, M. Niemier and **X. Hu**, "GC-eDRAM design using hybrid FinFET/NC-FinFET," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)* (ACM/IEEE), August 2020, pp. 199–204.

[C49] Q. Lou*, T. Gao, P. Faley, M. Niemier, **X. Hu** and S. Joshi, "Embedding error correction into crossbars for reliable matrix vector multiplication using emerging devices," *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)* (ACM/IEEE), August 2020, pp. 139–144.

[C50] A. Kazemi*, C. Alessandri, A. C. Seabaugh, **X. Hu**, M. Niemier and S. Joshi, "A device non-ideality resilient approach for mapping neural networks to crossbar arrays," *ACM/IEEE Design Automation Conference (DAC)* (ACM/IEEE), July 2020, pp. 1–6.

[C51] S. Mishra*, D. Chen and **X. Hu**, "A data-aware deep supervised method for retinal vessel segmentation," *IEEE International Symposium on Biomedical Imaging (ISBI)* (IEEE), April 2020, pp. 1254–1257.

[C52] K. Ni, A. Gupta, O. Prakash, S. Thomann, **X. Hu** and H. Amrouch, "Impact of extrinsic variation sources on the device-to-device variation in Ferroelectric FET," *IEEE International Reliability Physics Symposium (IRPS)* (IEEE), March 2020 (5 pages).

[C53] A. Gupta, K. Ni, O. Prakash, **X. Hu** and H. Amrouch, "Temperature dependence and temperature-aware sensing in Ferroelectric FET," *IEEE International Reliability Physics Symposium (IRPS)* (IEEE), March 2020 (5 pages).

[C54] D. Reis*, A.F. Laguna*, M. Niemier and **X. Hu**, "A fast and energy efficient Computing-in-Memory architecture for few-shot learning applications," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2020, pp. 127–132.

[C55] M.M. Sharifi*, R. Rajaei*, P. Cadareanu, P.-E. Gaillardon, Y. Jin, M. Niemier and **X. Hu**, "A novel TIGFET-based DFF design for improved resilience to power side-channel attacks," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2020, pp. 1253–1258.

[C56] M. Li*, X. Yin*, **X. Hu** and C. Zhuo, "Nonvolatile and energy-efficient FeFET-based multiplier for energy-harvesting devices," *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2020, pp. 562–567.

[C57] Y. Lin, Q. Zhang, J. Tang, B. Gao, C. Li, P. Yao, Z. Liu, J. Zhu, J. Lu, **X. Hu**, H. Qian and H. Wu, "Bayesian neural network realization by exploiting inherent stochastic behavior of analog RRAM," *IEEE International Electron Devices Meeting (IEDM)* (IEEE), 2019, pp. 14.6.1–14.6.4.

[C58] I. Palit*, Q. Lou*, R. Perricone*, M.Niemier and **X. Hu**, "A uniform modeling methodology for benchmarking DNN accelerators," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2019 (6 pages).

[C59] T. Gong, T. Zhang*, **X. Hu**, Q. Deng, M. Lemmon and S. Han, "Reliable dynamic packet scheduling over lossy real-time wireless network," *Euromicro Conference on Real-Time Systems (ECRTS)*, July 2019, pp. 11:1–11:23.

[C60] S. Mishra*, P. Liang, A. Czajka, D. Chen and **X. Hu**, "CC-Net: Image complexity guided network compression for biomedical image segmentation," *IEEE International Symposium on Biomedical Imaging (ISBI)* (IEEE), April 2019, pp. 57–60.

[C61] L. Li, T. Wei, J. Zhou*, M. Chen and **X. Hu**, "CE-based optimization for real-time system availability under learned soft error rate," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2019, pp. 1331–1336.

[C62] A. F. Laguna*, M. Niemier and **X. Hu**, "Design of hardware-friendly memory enhanced neural networks," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2019, pp. 1583–1586.

[C63] R. Perricone*, Z. Liang, M. G. Mankalale, M. Niemier, S. S. Sapatnekar, J.-P. Wang and **X. Hu**, "An energy efficient non-volatile flip-flop based on CoMET technology," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2019, pp. 390–395.

[C64] D. Zhang, Y. Ma*, C. Zheng, Y. Zhang, **X. Hu** and D. Wang, "Cooperative-competitive task allocation in edge computing for delay-sensitive social sensing," *ACM/IEEE Symposium on Edge Computing (SEC)* (ACM/IEEE), October 2018, pp. 243–259.

[C65] D. Reis*, M. Niemier and **X. Hu**, "Computing in-memory with FeFETs," *International Symposium on Low Power Electronics and Design (ISLPED)* (ACM/IEEE), July 2018. Article No. 24, pp. 1–6. (Received the **Best Paper** Award.)

[C66] X. Xu, Q. Lu, L. Yang, **X. Hu**, D.Z. Chen, Y. Hu and Y. Shi, "Quantization of fully convolutional networks for accurate biomedical image segmentation," *IEEE/CVF Conference on Computer Vision and Pattern Recognition (CVPR)* (IEEE), June 2018, pp. 8300–8308.

[C67] I. Palit*, L. Yang, Y. Ma*, D.Z. Chen, M. Niemier, J. Xiong and **X. Hu**, "Biomedical image segmentation using fully convolutional networks on TrueNorth," to *International Symposium on Computer-Based Medical Systems (CBMS)*, June 2018, pp. 375–380.

[C68] X. Chen*, Niemier and **X. Hu**, "Nonvolatile Lookup Table Design Based on Ferroelectric Field-Effect Transistors," *International Symposium on Circuits and Systems (ISCAS)* (IEEE), May 2018, pp. 1–5.

[C69] T. Zhang*, T. Gong, Z. Yun, S. Han, Q. Deng and **X. Hu**, "FD-PaS: A fully distributed packet scheduling framework for handling disturbances in real-time wireless networks," *IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)* (IEEE), April 2018, pp. 1–12.

[C70] D. Zhang, Y. Ma*, Y. Zhang, S. Lin, **X. Hu**, D. Wang, "A real-time and non-cooperative task allocation framework for social sensing applications in edge computing systems," *IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)* (IEEE), April 2018, pp. 316–326.

[C71] X. Chen*, X. Yin*, M. Niemier and **X. Hu**, "Design and optimization of FeFET-based crossbars for binary convolution neural networks," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2018, pp. 1211–1216.

[C72] X. Chen*, D.Z. Chen and **X. Hu**, "moDNN: Memory optimal DNN training on GPUs," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2018, pp. 13–18.

[C73] Y. Ma*, T. Chantem*, R. P. Dick, and **X. Hu**, "Improving reliability for real-time systems through dynamic recovery," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2018, pp. 521–526.

[C74] W. Chang, D. Roy, **X. Hu** and S. Chakraborty, "Cache-aware task scheduling for maximizing control performance," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2018, pp. 700–705.

[C75] L. Li, P. Cong, K. Cao, J. Zhou*, T. Wei, M. Chen and **X. Hu**, "Feedback control of real-time EtherCAT networks for reliability enhancement in CPS," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2018, pp. 694–699.

[C76] J. Zhou*, T. Wei, M. Chen, **X. Hu**, Y. Ma*, G. Zhang and J. Yan, "Variation-aware task allocation and scheduling for improving reliability of real-time MPSoCs," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2018, pp. 171–176.

[C77] X. Chen*, J. Chen, D.Z. Chen and **X. Hu**, "Optimizing memory efficiency for convolution kernels on Kepler GPUs," *Design Automation Conference (DAC)* (ACM/IEEE), June 2017, Article No. 68, 6 pages.

[C78] Y. Bai, **X. Hu**, R. F. DeMara and M. Lin, "A spin-orbit torque based Cellular Neural Network (CNN) architecture," *Great Lakes Symposium on VLSI (GLSVLSI)* (ACM), May 2017, pp. 59–64.

[C79] T. Zhang*, T. Gong, C. Gu, H. Ji, S. Han, Q. Deng and **X. Hu**, "Distributed dynamic packet scheduling for handling disturbances in real-time wireless networks," *IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)* (IEEE), April 2017, pp. 261–272.

[C80] J. Zhou*, J. Yan, T. Wei, M.Chen and **X. Hu**, "Energy-adaptive scheduling of imprecise computation tasks for QoS optimization in real-Ttme MPSoC systems," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2017, pp. 1402–1407.

[C81] Y. Ma*, T. Chantem*, R. Dick and **X. Hu**, "An on-line framework for improving reliability of real-time systems on 'Big-Little' type MPSoCs," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2017, pp. 446–451.

[C82] X. Yin*, M. Niemier and **X. Hu**, "Design and benchmarking of ferroelectric FET based TCAM," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2017, pp. 1444–1449.

[C83] X. Yin*, A. Aziz, J. Nahas, S. Datta, S. Gupta, M.Niemier and **X. Hu**, "Exploiting ferroelectric FETs for low-power non-volatile logic-in-memory circuits," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2016, pp. 121–126.

[C84] C. Gu*, N. Guan, Z.Feng, Q. Deng, **X. Hu** and Y. Wang, " Transforming real-time task graphs to improve schedulability," *IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA)* (IEEE), August 2016, pp. 29–38. (Nominated for the **Best Paper** Award.)

[C85] X. Yin*, B. Sedighi*, M. Niemier and **X. Hu**, "Design of latches and flip-flops using emerging tunneling devices," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2016, pp. 367–372.

[C86] T. Liu, H. Guo, S. Parameswaran and **X. Hu**, "Improving tag generation for memory data authentication in embedded processor systems," *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2016, pp. 50–55.

[C87] J. Zhou*, **X. Hu**, Y. Ma* and T. Wei, "Balancing lifetime and soft-error reliability to improve system availability," *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2016, pp. 685–690.

[C88] A. Tan, Q. Wang, N. Guan, Q. Deng and **X. Hu**, "Inter-cell channel time-slot scheduling for multichannel multiradio cellular fieldbuses," *IEEE real-time symposium (RTSS)* (IEEE), December 2015, pp. 227–238.

[C89] I. Palit*, Q. Lou, N. Acampora, J. Nahas, M.T. Niemier, **X. Hu**, "Analytically modeling power and performance of a CNN system," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2015, pp. 186–193.

[C90] K. Shamsi, Y. Bi, Y.Jin, P.-E. Gaillardon, M.Niemier and **X. Hu**. "Reliable and high performance STT-MRAM architectures based on controllable-polarity devices," *IEEE International Conference on Computer Design (ICCD)*, (IEEE), pp. 372–379, October 2015.

[C91] S. Arunachalam, T.Chantem*, R.P. Dick and **X. Hu**, "An online wear state monitoring methodology for off-the-shelf embedded processors," *International Conference on Hardware/Software Co-Design and System Synthesis (CODES+ISSS)* (IEEE), October 2015, pp. 114–123.

[C92] S. Hong*, **X. Hu**, T. Gong and S. Han, "On-line data link layer scheduling in wireless networked control systems," *Euromicro Conference on Real-Time Systems (ECRTS)*, pp. 57–66. July 2015.

[C93] K. Xiao*, D.Z. Chen, **X. Hu** and B. Zhou*, "Monte Carlo based ray tracing in CPU-GPU heterogeneous systems and applications in radiation therapy," *ACM Symposium on High-Performance Parallel and Distributed Computing (HPDC)*, (ACM), pp. 247–258, June 2015.

[C94] Y. Ma*, T. Chantem*, **X. Hu** and Robert P. Dick: "Improving lifetime of multicore soft real-time systems through global utilization control," *ACM Great Lakes Symposium on VLSI (GLVLSI)* (ACM), May 2015, pp. 79–82.

[C95] Q. Lou*, I. Palit*, A. Horvath, **X. Hu**, M. T. Niemier, J. Nahas, "TFET-based operational transconductance amplifier design for CNN systems," *ACM Great Lakes Symposium on VLSI (GLVLSI)* (ACM), May 2015, pp. 277–282.

[C96] A. Kiss, Z. Nagy, P. Szolgay, G. Csaba, **X. Hu** and W. Porod, "Emulating massively parallel non-Boolean operators on FPGA," *International Symposium on Circuits and Systems (ISCAS)* (IEEE), May 2015, pp. 1981–1984.

[C97] L. Tang*, **X. Hu**, R. Barrett, "PerDome: a performance model for heterogeneous computing systems," *High Performance Computing Symposium (HPC)*, (ACM), April 2015, pp. 225–232.

[C98] B. Sedighi*, I. Palit*, **X. Hu**, J. Nahas and Michael Niemier, "A CNN-inspired mixed signal processor based on tunnel transistors," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2015, pp. 1150–1155.

[C99] R. Perricone*, Y. Zhu*, K.M. Sanders*, **X. Hu** and M. Niemier, "Towards systematic design of 3D pNML layouts," *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2015, pp. 1539–1542.

Invited and Other Publications

[I1] **X. Hu**, M.-Y.Lee, M. Li, J.P.C. De Lima, L. Liu*, Z. Zhu, J. Castrillon, M. Niemier and Y. Wang, "Cross-layer design and design automation for in-memory computing based on non-volatile memory technologies," accepted to *IEEE Design & Test*, 2025.

[I2] S. Ullah, S. S. Sahoo, Can Li, Chao Li, L. Liu*, T. S. Pereira*, B. Wen, X. Yin, A. Darjani, N. Kavand, C. Bodla, R. Y. Panduga, A. Holemadlu, J. Maly, J. Förste, S. Vadia, **X. Hu**, and A. Kumar, "Invited Paper: Circuit and Architecture Design with Emerging Computing Paradigms," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), October 2025.

[I3] J. Henkel, L. Siddhu, H. Nassar, L. Bauer, J.-J. Chen, C. Hakert, T. Seidl, K. H. Chen, **X. Hu**, M. Li, C.-L. Yang, M.-L. Wei, "Co-designing NVM-based systems for machine learning and In-memory search applications," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), October 2024.

[I4] Y. Qin*, Z. Yan, W. Wen, **X. Hu** and Y. Shi, "Sustainable deployment of deep neural networks on non-volatile compute-in-memory accelerators" an **invited** paper, *International Conference on Hardware/Software Co-Design and System Synthesis (CODES+ISSS)* (ACM/IEEE), September 2024.

[I5] **X. Hu**, A. Girault and H. Falk, "Report on the 2023 Embedded Systems Week (ESWEEK)," *IEEE Design & Test*, Vol. 41, No. 2, 2024, pp. 84-87.

[I6] L. Liu*, A.F. Laguna, M. Niemier and **X. Hu**, "Design of high-performance and compact CAM for supporting data-intensive applications," *IEEE International Symposium on Circuits & Systems (ISCAS)* (IEEE), May 2024, pp. 1–5, doi: 10.1109/ISCAS58744.2024.10558698.

[I7] M. Niemier, Z. Enciso, M. Sharifi*, **X. Hu**, J. Castrillon, J.P.C. Lima, A.A. Khan, H. Fazaneh, I. O'Connor, N. Afroze, A. Khan, A. Graening, R. Sharima, P. Gupta and J. Rykaert, "Smoothing disruption across the stack: tales of memory, heterogeneity, & compilers," an **invited** paper, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2024, pp. 1–10, doi: 10.23919/DATE58400.2024.10546772.

[I8] Z. Yan*, Y. Qin, **X. Hu** and Y. Shi, "On the viability of using LLMs for SW/HW co-design: an example in designing CiM DNN accelerators," an **invited** paper, *IEEE International System-on-Chip Conference (SOCC)* (IEEE), November 2023.

[I9] M. Niemier, **X. Hu**, L. Liu*, M. Sharifi*, I. O'Connor, D. Atienza, G. Ansaloni, C. Li, A. Khan and D. C. Ralph, "Cross-layer design for the predictive assessment of technology-enabled architectures," an **invited** paper, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), April 2023.

[I10] A. Shrivastava and **X. Hu**, "Report on the 2022 Embedded Systems Week (ESWEEK)," *IEEE Design & Test*, Vol. 40, No. 1, pp. 108–111, February 2023.

[I11] D. Reis, A. F. Laguna, M. Niemier and **X. Hu**, "In-memory computing accelerators for emerging learning paradigm," an **invited** paper, *Asia and South Pacific Design Automation Conference (ASPDAC)* (IEEE), January 2023, pp. 606–611.

[I12] D. Reis, A. F. Laguna, M. Li*, M. Niemier and **X. Hu**, "Ferroelectric FET configurable memory arrays and their applications," an **invited** paper, *IEEE International Electron Devices Meeting (IEDM)* (IEEE), December 2022.

[I13] R. Ernst and **X. Hu**, "Autonomous systems design — a virtual roundtable," *IEEE Computer*, Vol. 54, No. 11, pp. 17–25, November 2021.

[I14] X. Guo, S. Han, **X. Hu**, X. Jiao, Y. Jin, F. Kong and M. Lemmon, "Towards scalable, secure, and smart mission-critical IoT systems: review and vision: (Special Session Paper)," *International Conference on Embedded Software* (ACM/IEEE), October 2021, pp. 1–10.

[I15] **X. Hu**, M. Niemier, A. Kazemi*, A. F. Laguna*, K. Ni, R. Rajaei*, M. M. Sharifi* and X. Yin, "In-memory computing with associative memories: a cross-layer perspective," an **invited** paper, *IEEE International Electron Devices Meeting (IEDM)* (IEEE), December 2021, pp. pp. 25.2.1–25.2.4.

[I16] H. Amrouch, D. Gao , **X. Hu**, A. Kazemi*, A. F. Laguna*, K. Ni, M. Niemier, M. M. Sharifi*, S. Thomann, X. Yin and C. Zhuo, "ICCAD tutorial session paper: Ferroelectric FET technology and applications: from devices to systems," *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2021.

[I17] D. Reis*, A.F. Laguna*, M. Niemier and **X. Hu**, "Exploiting FeFETs via cross-layer design from in-memory computing circuits to meta-learning applications," an **invited** paper, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2021, pp. 306–311.

[I18] H. Amrouch, **X. Hu**, M. Imani, A. Laguna*, M. Niemier, S. Thomann, X. Yin* and C. Zhuo, "Cross-layer design for Computing-in-Memory: From Devices,Circuits, to Architectures and Applications," an **invited** paper, *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2021, pp. 132–139.

[I19] Z. Yan*, D.-C. Juan, **X. Hu** and Y. Shi, "Uncertainty modeling of emerging device based computing-in-memory neural accelerators with application to neural architecture search," an **invited** paper, *Asia and South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), January 2021, pp. 859–864.

[I20] D. Ma, X. Yin*, M. Niemier, **X. Hu** and X. Jiao, "AxR-NN: Approximate computation reuse for energy-efficient convolutional neural networks," an **invited** paper, *Great Lakes VLSI Symposium (GLVLSI)* (ACM), September 2020, pp. 363–368.

[I21] D. Reis*, D. Gao, X. Yin, D. Fan, M. Niemier, C. Zhuo and **X. Hu**, "Modeling and benchmarking computing-in-memory for design space exploration," an **invited** paper, *Great Lakes VLSI Symposium (GLVLSI)* (ACM), September 2020, pp. 39–44.

[I22] Z. Zhu, H. Sun, K. Qiu, L. Xia, G. Krishnan, G. Dai, D. Niu, X. Chen, **X. Hu**, Y. Cao, Y. Xie, Y. Wang and H. Yang, "MNSIM 2.0: A behavior-level modeling tool for memristor-based neuromorphic computing systems," an **invited** paper, *Great Lakes VLSI Symposium (GLVLSI)* (ACM), September 2020, pp. 83–88.

[I23] D. Brooks, T. Gokmen, U. Gupta, **X. Hu**, S. Jain, A.F. Laguna*, M. Niemier, A. Raghunathan, A. Ranjan, D. Reis*, J. Stevens, C-J. Wu and X. Yin*, "Emerging neural workloads and their impact on hardware," an **invited** paper, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2020, pp. 1462–1471.

[I24] J. Henkel, H. Amrouch, M. Rapp, S. Salamin, D. Reis*, D. Gao, X. Yin*, M. Niemier, C. Zhuo, **X. Hu**, H.-Y. Cheng, C.-L. Yang, "The impact of emerging technologies on architectures and system-level management," an **invited** paper, *International Conference on Computer-Aided Design (ICCAD)* (ACM/IEEE), November 2019, pp. 794–799.

[I25] S. Angizi, Z. He, D. Reis*, **X. Hu**, W. Tsai, S. J. Lin and D. Fan, "Accelerating deep neural networks in processing-in-memory platforms: analog or digital approach?" an **invited** paper, *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)* (IEEE), 2019, pp. 197–202.

[I26] X. Yin*, D. Reis*, M. Niemier and **X. Hu**, "Ferroelectric FET based TCAM designs for energy efficient computing" an **invited** paper, *IEEE Computer Society Annual Symposium on VLSI (ISVLSI)* (IEEE), July 2019, pp. 437–442.

[I27] A.F. Laguna*, X. Yin*, D. Reis*, M. Niemier and **X. Hu**, "Ferroelectric FET based In-memory computing," an **invited** paper, *Great Lakes VLSI Symposium (GLVLSI)* (ACM), May 2019, pp. 373–378.

[I28] **X. Hu**, R. Ernst, P. Eles, G. Heiser, K. Keutzer, D. Kim and T. Tohdo, "Roundtable: Machine learning for embedded systems: hype or lasting impact?" *IEEE Design & Test*, Vol. 35, No. 6, pp. 86–93, 2018.

[I29] S. Rai, S. Srinivasa, P. Cadareanu, X. Yin*, **X. Hu**, P.-E. Gaillardon, V. Narayanan and A. Kumar, "Emerging reconfigurable nanotechnologies: can they support future electronics?" an **invited** paper, *International Conference on Computer-Aided Design (ICCAD)* (ACM/IEEE), November 2018, Article 13, 8 pages.

[I30] A. Aziz, E.T. Breyer, A. Chen, X. Chen*, S. Datta, S.K. Gupta, M. Hoffmann, **X. Hu**, A. Ionescu, M. Jerry, T. Mikolajick, H.Mulaosmanovic, K. Ni, M. Niemier, I. O'Connor, A. Saha, S. Slesazeck, S.K. Thirumala and X. Yin*, "Computing with ferroelectric FETs: Devices, models, systems, and applications," an **invited** paper, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2018, pp. 1295-1304.

[I31] X. Yin*, Z Toroczkai and **X. Hu**, "An analog SAT solver based on a deterministic dynamical system," an **invited** paper, *International Conference on Computer-Aided Design (ICCAD)* (ACM/IEEE), November 2017, pp. 794–799.

[I32] X. Xu, Q. Lu, T. Wang, J. Liu, C. Zhuo, **X. Hu** and Y. Shi, "Edge Segmentation: Empowering mobile telemedicine with compressed cellular neural networks," an **invited** paper, *International Conference on Computer-Aided Design (ICCAD)* (ACM/IEEE), November 2017, pp. 880–887.

[I33] R. Perricone*, M. Niemier, and **X. Hu**, an **invited** paper, "Challenges and opportunities with spin-based logic," *SPIE 10357, Spintronics X*, 2017, pp. 103570M.

[I34] J.-P. Wang, S. S. Sapatnekar, C. H. Kim, P. Crowell, S. Koester, S. Datta, K. Roy, A. Raghunathan, **X. Hu**, M. Niemier, A. Naeemi, C.-L. Chien, C. Ross and R. Kawakami, "A pathway to enable exponential scaling for the beyond-CMOS era," an **invited** paper, *Design Automation Conference (DAC)* (ACM/IEEE), June 2017, Article 16, 6 pages.

[I35] R. Perricone*, L. Tang*, M. Niemier and **X. Hu**, "Exploiting non-volatility for information processing," an **invited** paper, *Great Lakes VLSI Symposium (GLVLSI)* (ACM), May 2017, pp. 305–310.

[I36] A. Horvath, M. Hillmer, Q. Lou*, **X. Hu** and M. Niemier, "Cellular neural network friendly convolutional neural networks – CNNs with CNNs," an **invited** paper, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2017, pp. 145-150.

[I37] R. Perricone*, I. Ahmed, Z. Liang, M.G. Mankalaley **X. Hu**, C. H. Kim, M.Niemier, S.S. Sapatnekar and J-P Wang, "Advanced spintronic memory and logic for non-volatile processors," an **invited** paper, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2017, pp. 972-977.

[I38] J. Wu, J. Liu, **X. Hu** and Y. Shi, "Privacy protection via appliance scheduling in smart homes," an **invited** paper, *International Conference on Computer-Aided Design (ICCAD)* (ACM/IEEE), November 2016, pp. 106–111.

[I39] S. Hu, **X. Hu** and A. Zomaya, "Leveraging design automation techniques for cyber-physical system design," **Guest Editorial**, *IEEE Transactions on CAD of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 35, No 5, 2016, pp. 697–698.

[I40] A. Chen, **X. Hu**, Y. Jin, M. Niemier and X. Yin*, "Enhancing hardware security with emerging transistor technologies," an **invited** paper, *ACM Great Lakes Symposium on VLSI (GLVLSI)* (ACM), May 2016, pp. 305–310.

[I41] R. Perricone*, **X. Hu**, J. Nahas, and M. Niemier, "Can beyond-CMOS devices illuminate dark silicon?" an **invited** paper, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2016, pp. 13–18.

[I42] A. Chen, **X. Hu**, Y. Jin, M. Niemier and X. Yin*, "Using emerging technologies for hardware security beyond PUFs," an **invited** paper, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2016, pp. 1544–1549.

[I43] M.T. Niemier and **X. Hu**, "Potential benefits from image processing hardware based on emerging transistor technologies," an **invited** paper, *International Society for Optics and Photonics (SPIE) Newsroom*, June 2015.