

## Complete Publication List of Xiaobo Sharon Hu

### Book Chapters

- [B1] Z. Yan\*, Q. Lu, Weiwen Jiang, Lei Yang, **X. Hu**, Jingtong Hu and Y. Shi, “Hardware–Software Co-design of Deep Neural Architectures: From FPGAs and ASICs to Computing-in-Memories,” *Embedded Machine Learning for Cyber-Physical, IoT, and Edge Computing*, S. Pasricha and M. Shafique (Eds.), Springer, Cham, 2024, pp. 271–301.
- [B2] Z. Yan\*, **X. Hu** and Y. Shi, “On the Reliability of Computing-in-Memory Accelerators for Deep Neural Networks,” *System Dependability and Analytics*, L. Wang, K. Pattabiraman, C. Di Martino, A. Athreya, S. Bagchi (Eds.), Springer, Cham, 2023, pp. 167–190.
- [B3] T. Zhang\*, G. Tao, **X. Hu**, Q. Deng and S. Han, “Dynamic Resource Management in Real-Time Wireless Networks,” *Wireless Networks and Industrial IoT*, N.H. Mahmood, N. Marchenko, M. Gidlund, P. Popovski (Eds.), Springer, 2021, pp. 131–156.
- [B4] Y. Ma\*, J. Zhou, T. Chantem\*, R. P. Dick, and **X. Hu**, “Resource Management for Improving Overall Reliability of Multi-Processor Systems-on-Chip,” *Dependable Embedded Systems*, J. Henkel and N. Dutt (Eds.), Springer International Publishing, 2021, pp. 233–246.
- [B5] Y Bi, P.-E. Gaillardon, **X. Hu**, M. Niemier, J.-S. Yuan and Y. Jin, “Polarity-Controllable Silicon NanoWire FET-Based Security,” *Security Opportunities in Nano Devices and Emerging Technologies*, M. Tehranipoor, D. Forte, G.S. Rose, S. Bhunia (Eds.), Taylor & Francis, 2017, pp. 165–178.
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- [B9] Y. Zhang\*, **X. Hu** and D.Z. Chen, “Energy Minimization in Multiprocessor Real-Time Systems,” *Handbook of Energy-Aware and Green Computing*, I. Ahmad and S. Ranka (Eds.), CRC Press, January 2012, pp 519–542.
- [B10] G. Quan\* and **X. Hu**, “Minimum Energy Fixed-Priority Scheduling for Variable Voltage Processors,” *Design, Automation, and Test in Europe – The Most Influential Papers of 10 Years DATE*, R. Lauwereins and J. Madsen (Eds.), Springer, March 2008, pp. 313–324.

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\*Student or postdoctoral fellow advised or co-advised by X. Sharon Hu.

- [B11] **X. Hu** and G. Quan\*, “Fundamentals of Power-Aware Scheduling,” *Embedded Processor and System Design – A Low Power Perspective*, J. Henkel and S. Parameswaran (Eds.), Kluwer Academic Publishers, 2007, pp. 219–229.
- [B12] G. Quan\* and **X. Hu**, “Static DVFS Scheduling,” *Embedded Processor and System Design – A Low Power Perspective*, J. Henkel and S. Parameswaran (Eds.), Kluwer Academic Publishers, 2007, pp. 231-242.
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### Refereed Journal Articles (published or accepted for publication)

- [J1] F.-X. Liang\*, S. Kumar, K. Ni, W. Chakraborty, Y. Chauhan, H. Amrouch, S. Datta, M. T. Niemier and **X. Hu**, “A physics-based model for oxide-semiconductor-based ferroelectric field-effect transistors,” accepted to *IEEE Transactions on Electronic Devices (IEEE TED)*, 2024.
- [J2] R. Wang, S. H. Moon, **X. Hu**, X. Jiao and D. Reis, “A computing-in-memory-based one-class hyperdimensional computing model for outlier detection,” accepted to *IEEE Transactions on Computers (IEEE TC)*, 2024.
- [J3] Z. Yan\*, **X. Hu** and Y. Shi, “Compute-in-memory based neural network accelerators for safety-critical systems: worst-case scenarios and protections,” accepted to *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, 2024.
- [J4] Z. Yan\*, **X. Hu** and Y. Shi, “U-SWIM: Universal Selective Write-Verify for computing-in-memory neural accelerators,” accepted to *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, 2024.
- [J5] Y. Xu, Z. Zhao, Y. Xiao, T. Yu, H. Mulaosmanovic, D.Kleimaier, S. Duenkel, S. Beyer, X. Gong, R. Joshi, **X. Hu**, S. Wen, A.S. Rios, K. Lekkala, L. ItItti, E. Homan, S. George, V. Narayanan and K. Ni, “Ferroelectric FET based context-switching FPGA enabling dynamic reconfiguration for adaptive deep learning machines,” accepted to *Science Advances*, 2023.
- [J6] X. Yang, Z. Wang, **X. Hu**, C. H. Kim, S. Yu, M. Pajic, R. Manohar, Y. Chen and H. Li, “Neuro-symbolic computing: advancements and challenges in hardware-software co-design”, accepted to *IEEE Transactions on Circuits and Systems II (TCAS-II)*, 2023.
- [J7] J. Takeshita, D. Reis\*, T. Gong, M. T. Niemier, **X. Hu** and T. Jung, “Accelerating Finite-Field and Torus FHE via Compute-Enabled (S)RAM,” Special Issue on Near / In-Memory Processing, accepted to *IEEE Transactions on Computers (IEEE TC)*, 2023.
- [J8] T. Zhang\*, T. Gong, M Lyu, N Guan, S Han and **X. Hu**, “Reliable dynamic packet scheduling with slot sharing for real-time wireless networks,” *IEEE Transactions on Mobile Computing (IEEE TMC)*, Vol. 22, No. 11, 2023, pp. 6723–6741.

- [J9] J. Gong, H. Saadat, H. Gamaarachchi, H. Javaid, **X. Hu** and S. Parameswaran, “ApproxTrain: Fast simulation of approximate multipliers for DNN training and inference,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 42, No. 11, 2023, pp. 3505–3518.
- [J10] Z. Zhe, H. Sun, T. Xie, Y. Zhu, G. Dai, L. Xia, D. Niu, X. Chen,, **X. Hu** , Y. Cao, Y. Xie, H. Yang and Y. Wang, “MNSIM 2.0: A behavior-level modeling tool for processing-in-memory architectures,” *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 42, No. 11, 2023, pp. 4112–4125.
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## Refereed Conference Papers (published or accepted for publication)

- [C1] H. Farzaneh, J. P. Cardoso De Lima, M Li\*, A. A. Khan, **X. Hu** and J. Castrillon, “C4CAM: A Compiler for CAM-based In-memory Accelerators,” *ACM International Conference on Architectural Support for Programming Languages and Operating System (ASPLOS)* (ACM), April 2024, Volume 3.
- [C2] T. Zhang, J. Wang, **X. Hu** and S. Han, “Real-time flow scheduling in industrial 5G new radio,” *IEEE real-time symposium (RTSS)* (IEEE), December 2023, pp. 371–384.
- [C3] J. Wang, T. Zhang, Q. Deng, **X. Hu** and S. Han, “Resource virtualization with end-to-end timing guarantees for multi-hop multi-channel real-time wireless networks,” *IEEE real-time symposium (RTSS)* (IEEE), December 2023, pp. 385–396.
- [C4] M Li\*, H. Geng\*, M. Niemier and **X. Hu**, “Accelerating polynomial modular multiplication with crossbar-based compute-in-memory,” *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2023, pp. 1–9.
- [C5] Z. Yan\*, Y. Qin, W. Wen, **X. Hu** and Y. Shi, “Improving realistic worst-case performance of NVCiM DNN accelerators through training with right-censored Gaussian noise,” *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2023, pp. 1-9. (Received the **William J. McCalla ICCAD Best Paper** Award.)
- [C6] S. Shou, C. Liu, S. Yun, Z. Wan, K. Ni, M. Imani, **X. Hu**, J. Yang, C. Zhuo and X. Yin, “SEE-MCAM: Scalable multi-bit FeFET content addressable memories for energy efficient associative search,” *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2023, pp. 1-9.
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- [C9] M. Li\*, A. Kazemi\*, A. F. Laguna\* and **X. Hu**, “Associative memory based experience replay for deep reinforcement learning,” *International Conference on Computer Aided Design (ICCAD)* (ACM/IEEE), November 2022. Article No. 135, pp. 1–9.
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- [I4] Z. Yan\*, Y. Qin, **X. Hu** and Y. Shi, “On the viability of using LLMs for SW/HW co-design: an example in designing CiM DNN accelerators,” an **invited** paper, *IEEE International System-on-Chip Conference (SOCC)* (IEEE), November 2023.
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