CURRICULUM VITAE

Xiaobo Sharon Hu
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Current Position

Leo E. and Patti Ruth Linbeck Professor of Engineering in the Department of Computer Science and Engineering and Concurrent Professor in the Department of Electrical Engineering at University of Notre Dame, Notre Dame, Indiana, USA.

Education

Ph.D.	Electrical Engineering, December 1989 Purdue University, West Lafayette, Indiana
M.S.	Electrophysics, May 1984 Polytechnic Institute of New York, Brooklyn, New York
B.S.	Engineering, July 1982 Tianjin University, Tianjin, P.R. China

Awards and Honors

- Rev. James A. Burns, C.S.C., Award, University of Notre Dame, 2026. (The award recognizes outstanding faculty as doctoral advisers.)
- Distinguished Service Award, ACM Special Interest Group on Design Automation (SIGDA), 2025.
- Outstanding Technical Achievement and Leadership Award, IEEE Technical Community on Real-Time Systems (TC-RTS), 2024.
- Distinguished Leadership Award, IEEE Technical Community on Cyber-Physical Systems (TC-CPS), 2024.
- Best Paper Award Candidate, *IEEE/ACM International Conference on Computer Aided Design (ICCAD)*, 2024.
- Outstanding Service Recognition Award, IEEE Council of Electronic Design Automation, 2024.
- William J. McCalla ICCAD Best Paper Award, *ACM/IEEE International Conference on Computer Aided Design (ICCAD)*, 2023. (Two papers received the award out of 750 papers.)
- Marie R. Pistilli Women in Engineering Achievement Award, 2023.
- Fellow of the Asia-Pacific Artificial Intelligence Association (AAIA), 2022.
- Fellow of the Association for Computing Machinery (ACM), Class of 2021.
- Best Paper Nomination, *IEEE VLSI Test Symposium (VTS)* (IEEE), 2021.
- Best Paper Nomination, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), 2021.
- Outstanding Service Recognition Award, IEEE Council of Electronic Design Automation, 2019.
- Distinguished Lecturer, *IEEE Council of Electronic Design Automation*, 2018–2021.
- Best Paper Award, *ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED)*, 2018.
- Fellow of the Institute of Electrical and Electronics Engineers (IEEE), Class of 2016.
- Best Paper Nomination, *IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA)*, 2016.
- Best Paper Nomination, *Asia and South Pacific Design Automation Conference (ASPDAC)*, 2013.

- Best Paper Nomination, *International Conference on Compilers, Architectures and Synthesis for Embedded Systems (CASES)*, 2012.
- Best Paper Nomination, *IEEE Symposium on Application Specific Processors (SASP)*, 2011.
- Best Paper Award, *IEEE Symposium on Nanoscale Architectures (NANOARCH)*, 2009.
- The Most Influential Papers of 10 Years, *Design, Automation, and Test in Europe Conference (DATE)*, 2007. (DATE is a premiere conference in Electronic Design Automation. Three papers were selected from over 200 papers in each annual proceedings between 1998-2007.)
- Best Paper Award, *38th ACM/ IEEE Design Automation Conference (DAC)*, 2001. (DAC is the premiere conference in Electronic Design Automation and the Best Paper award was selected from over 400 submissions).
- Recognition of Service Award, ACM, 2002.
- CAREER (Early Career Development) Award, the National Science Foundation (NSF), 1997.
- One of the two nominees for the National Science Foundation Presidential Faculty Fellows Award, Western Michigan University, 1996.

Professional Experience

07/2024–present: Leo E. and Patti Ruth Linbeck Professor of Engineering, Department of Computer Science and Engineering (with a concurrent appointment at Dept. of Electrical Engineering), University of Notre Dame, Notre Dame, Indiana.

05/2026–06/2026: Visiting Professor, Institute of Electrical and Micro Engineering, EPFL – Swiss Federal Technology Institute of Lausanne, Lausanne, Switzerland.

03/2026–04/2026: Visiting Chair Professor, College of Electrical Engineering and Computer Science, National Taiwan University, Taipei, Taiwan.

01/2026–02/2026: Visiting Researcher, School of Electrical and Computer Engineering, University of Sydney, Sydney, Australia.

11/2022–11/2025: Program Director (on Intergovernmental Personnel Act assignment), Division of Computing and Communication Foundations (CCF), Directorate of Computer and Information Science and Engineering (CISE), National Science Foundation, Alexandria, Virginia.

08/2008–06/2024: Professor, Department of Computer Science and Engineering (with a concurrent appointment at Dept. of Electrical Engineering), University of Notre Dame, Notre Dame, Indiana.

08/2022–11/2022: Visiting Professor, NeuroCore Group, EMD Electronics, San Jose, California.

12/2018–02/2019: Visiting Professorial Fellow, Department of Computer Science and Engineering, University of New South Wales, Sydney, Australia.

08/2018–12/2018, 03/2019–08/2019: Visiting Professor, Institute of Microelectronics, Tsinghua University, Beijing, China.

04/2012–05/2012: Visiting Professor, College of Computer Science and Technology, Zhejiang University, Hangzhou, China.

01/2012–03/2012: Visiting Professor, Department of Electronic Engineering, Tsinghua University, Beijing, China.

08/2000–08/2008: Associate Professor, Department of Computer Science and Engineering with tenure, University of Notre Dame, Notre Dame, Indiana.

01/2003–07/2003: Visiting Associate Professor, Department of Electrical and Electronic Engineering, Hong Kong University of Science and Technology (HKUST), Hong Kong.

08/1996–08/2000: Assistant Professor, Department of Computer Science and Engineering, University of Notre Dame, Notre Dame, Indiana.

08/1993–08/1996: Assistant Professor, Department of Electrical and Computer Engineering, with a joint appointment from the Department of Computer Science, Western Michigan University, Kalamazoo, Michigan.

12/1989–08/1993: Senior Research Engineer, Department of Electrical and Electronic Engineering, General Motors Research Laboratories, Warren, Michigan.

10/1984–08/1985: Design Engineer, IC Design Center, Delco Electronics, Kokomo, Indiana.

Areas of Research Interest

- Energy and reliability aware system-level design
- Circuit and architecture design with CMOS and beyond-CMOS devices
- Algorithm and hardware co-design for machine learning, medical, and privacy-preserving applications
- Design and analysis of embedded and real-time systems
- Computer-aided design of VLSI circuits and systems

Book Chapters

[B1] Z. Yan[*], Q. Lu, Weiwen Jiang, Lei Yang, **X. Hu**, Jingtong Hu and Y. Shi, "Hardware–Software Co-design of Deep Neural Architectures: From FPGAs and ASICs to Computing-in-Memories," *Embedded Machine Learning for Cyber-Physical, IoT, and Edge Computing*, S. Pasricha and M. Shafique (Eds.), Springer, Cham, 2024, pp. 271–301.

[B2] Z. Yan*, **X. Hu** and Y. Shi, "On the Reliability of Computing-in-Memory Accelerators for Deep Neural Networks," *System Dependability and Analytics*, L. Wang, K. Pattabiraman, C. Di Martino, A. Athreya, S. Bagchi (Eds.), Springer, Cham, 2023, pp. 167–190.

[B3] T. Zhang, G. Tao, **X. Hu**, Q. Deng and S. Han, "Dynamic Resource Management in Real-Time Wireless Networks," *Wireless Networks and Industrial IoT*, N.H. Mahmood, N. Marchenko, M. Gidlund, P. Popovski (Eds.), Spinger, 2021, pp. 131–156.

[B4] Y. Ma*, J. Zhou, T. Chantem, R. P. Dick, and **X. Hu**, "Resource Management for Improving Overall Reliability of Multi-Processor Systems-on-Chip," *Dependable Embedded Systems*, J. Henkel and N. Dutt (Eds.), Springer International Publishing, 2021, pp. 233–246.

[B5] Y. Bi, P.-E. Gaillardon, **X. Hu**, M. Niemier, J.-S. Yuan and Y. Jin, "Polarity-Controllable Silicon NanoWire FET-Based Security," *Security Opportunities in Nano Devices and Emerging Technologies*, M. Tehranipoor, D. Forte, G.S. Rose, S. Bhunia (Eds.), Tayor & Francis, 2017, pp. 165–178.

[*]Student or postdoctoral fellow advised or co-advised by X. Sharon Hu at the time of publication.

[B6] G. Csaba, G.H. Bernstein, A. Orlov, M.T. Niemier, **X. Hu** and W. Porod, "Nanomagnetic logic: from magnetic ordering to magnetic computing," *CMOS and Beyond: Logic Switches for Terascale Integrated Circuits*, T.-J.K. Liu, K.J. Kuhn (Eds.), Cambridge University Press, 2015, pp. 301–334.

Refereed Journal Articles (published or accepted for publication)

[J1] B. Wen, G. Gao, Z. Xu, M. Jiang, R. Mao, X. Qi, J. Chen, X. Yin, **X. Hu** and C. Li, "Trustworthy tree-based machine learning by MoS_2 flash-based analog content addressable memory with inherent soft boundaries," *Nature Communications*, 17, 5684, 2026.

[J2] Z. M. Enciso, J. Liu, B. Cheng, L. Pei, S. Davis, Y. Qin*, Z. Jia, X. Hu, Y. Shi, M. Niemier and N. Cao, "A 350pW implantable ventricular arrhythmia detection engine with Bayesian uncertainty quantification in 65nm CMOS," accepted to *IEEE Journal of Solid-State Circuits*, 2026.

[J3] A. Vardar, N. Laleni, S. Baskaran, M. Sharifi*, F. Mueller, J. Chandler, C. Zhuo, X. Yin, M. Niemier, B. Li, **X. Hu**, K. Seidel, K. Ni, and T. Kämpfe, "A 28nm FeFET-based content-addressable memory for energy-efficient similarity search and few-shot learning," accepted to *IEEE Journal of the Electron Devices Society (JEDSS)*, 2025

[J4] L. Liu*, M. Sharifi*, K. Wang, R. Mao, K. Ni, C. Li, X. Yin, M. Niemier and **X. Hu**, "EvaCAM: A circuit-level evaluation tool for general content addressable memories," accepted to *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, 2025.

[J5] G. Meng*, R. Zhou, L. Liu*, P. Liang, F. Liu, D.Z. Chen, M. Niemier and **X. Hu**, "Efficient approximation of earth mover's distance based on nearest neighbor search," *IEEE Transactions on Multimedia (IEEE TMM)*, Vol. 28, pp. 227–240, 2026.

[J6] H. Geng*, J. Mo, D. Reis 3, J. Takeshita, T. Jung, B. Reagen, M.Niemier and **X. Hu**, "PPIMCE: An in-memory computing fabric for privacy preserving computing," JCST 40th Anniversary Special Issue, *Journal of Computer Science and Technology (JCST)*, pp. 83–102, 2026.

[J7] Y. Qin*, Z. Yan, W. Wen, **X. Hu** and Y. Shi, "NeFT: Negative feedback training to improve robustness of Compute-In-Memory DNN accelerators," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 45, No. 2, 2026, pp. 983-997.

[J8] P. Liang, Y. Ding, Y. Zhang, J. Chen, H. Zheng, H. Wang, Y. Zhang, G. Meng, T. Weninger, **X. Hu** and D.Z. Chen, "Cell instance segmentation: the devil Is in the boundaries," *IEEE Transactions on Medical Imaging (IEEE TMI)*, Vol. 45, No. 4, 2026, pp. 1311–1324.

[J9] T. Zhang, J. Wang, **X. Hu** and S Han, "5G-TPS: A two-phase real-time scheduling and adaptation framework for 5G radio access networks," *IEEE Transactions on Mobile Computing (IEEE TMC)*, Vol. 25, No. 1, 2026, pp. 1320–1336.

[J10] X. Niu, S. Deng, F.-X. Liang*, K. A. Aabrar, Y. Qin, J. Duan, S. Datta, V. Narayanan, **X. Hu** and K. Ni, "Forming process in BEOL oxide channel ferroelectric FET," *IEEE Transactions on Electron Devices IIEEE TED)*, Vol. 72, No. 12, 2025, pp. pp. 6963–6969.

[J11] A. Mamdouh, H. Geng*, M. Niemier, **X. Hu** and D. Reis, "Shared-PIM: enabling concurrent computation and data flow for faster processing-in-DRAM," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 44, No. 11, 2025, pp. 4395–4404.

[J12] X. Yin, Q. Huang, H. E. Barkam, F. Müller, S. Deng, A. Vardar, S. De, Z. Jiang, M. Imani, U. Schlichtmann, **X. Hu**, C. Zhuo, T. Kämpfe and K. Ni, "A homogeneous FeFET-based time-domain compute-in-memory fabric for matrix-vector multiplication and associative search," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 44, No. 5, 2025, pp. 1856–1868.

[J13] M. Li*, D. Reis, A. F. Laguna, M. Niemier and **X. Hu**, "Accelerating recommendation systems with in-memory embedding operations," *IEEE Transactions on Circuits and Systems for Artificial Intelligence (IEEE TCAS-AI)*, Vol. 1, No. 2, 2024, pp. 244–256.

[J14] Z. Yan*, **X. Hu** and Y. Shi, "U-SWIM: Universal Selective Write-Verify for computing-in-memory neural accelerators," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 43, No. 6, 2024, pp. 1822–1833.

[J15] F.-X. Liang*, S. Kumar, K. Ni, W. Chakraborty, Y. Chauhan, H. Amrouch, S. Datta, M. T. Niemier and **X. Hu**, "A physics-based model for oxide-semiconductor-based ferroelectric field-effect transistors," *IEEE Transactions on Electronic Devices (IEEE TED)*, Vol. 71, No. 7, 2024, pp. 4397-4402.

[J16] X. Yin, F. Müller, A. F. Laguna, C. Li, Q. Huang, Z. Shi, M. Lederer, N. Laleni, S. Deng, Z. Zhao, M. Imani, Y. Shi, M. Niemier, **X. Hu**, C. Zhuo, T. Kämpfe and K. Ni, "Deep random forest with ferroelectric analog content addressable memory," *Science Advances*, 10(23), 2024, eadk8471.

[J17] Z. Yan*, **X. Hu** and Y. Shi, "Compute-in-memory based neural network accelerators for safety-critical systems: worst-case scenarios and protections," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 43, No. 8, 2024, pp. 2452-2464.

[J18] Y. Xu, Z. Zhao, Y. Xiao, T. Yu, H. Mulaosmanovic, D.Kleimaier, S. Duenkel, S. Beyer,X. Gong, R. Joshi, **X. Hu**, S. Wen, A.S. Rios, K. Lekkala, L. ItItti, E. Homan, S. George,V. Narayanan and K. Ni, "Ferroelectric FET based context-switching FPGA enabling dynamic reconfiguration for adaptive deep learning machines," *Science Advances*, 10(3), 2024, eadk1525.

[J19] X. Yang, Z. Wang, **X. Hu**, C. H. Kim, S. Yu, M. Pajic, R. Manohar, Y. Chen and H. Li, "Neuro-symbolic computing: advancements and challenges in hardware-software co-design", *IEEE Transactions on Circuits and Systems II (TCAS-II)*, Vol. 71, No. 3, 2024, pp. 1683-1689.

[J20] J. Takeshita, D. Reis*, T. Gong, M. T. Niemier, **X. Hu** and T. Jung, "Accelerating Finite-Field and Torus FHE via Compute-Enabled (S)RAM," Special Issue on Near / In-Memory Processing, *IEEE Transactions on Computers (IEEE TC)*, Vol. 73, No. 10, 2024, pp. 2449-2462.

[J21] R. Wang, S. H. Moon, **X. Hu**, X. Jiao and D. Reis, "A computing-in-memory-based one-class hyperdimensional computing model for outlier detection," *IEEE Transactions on Computers (IEEE TC)*, Vol. 73, No. 6, 2024, pp. 1559-1574.

[J22] T. Zhang, T. Gong, M Lyu, N Guan, S Han and **X. Hu**, "Reliable dynamic packet scheduling with slot sharing for real-time wireless networks," *IEEE Transactions on Mobile Computing (IEEE TMC)*, Vol. 22, No. 11, 2023, pp. 6723–6741.

[J23] J. Gong, H. Saadat, H. Gamaarachchi, H. Javaid, **X. Hu** and S. Parameswaran, "ApproxTrain: Fast simulation of approximate multipliers for DNN training and inference," *IEEE Transactions*

on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD), Vol. 42, No. 11, 2023, pp. 3505-3518.

[J24] Z. Zhe, H. Sun, T. Xie, Y. Zhu, G. Dai, L. Xia, D. Niu, X. Chen,, **X. Hu** , Y. Cao, Y. Xie, H. Yang and Y. Wang, "MNSIM 2.0: A behavior-level modeling tool for processing-in-memory architectures," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 42, No. 11, 2023, pp. 4112–4125.

[J25] Z. Jia, J. Chen, X. Xu, J. Kheir, J. Hu, H. Xiao, S. Peng, **X. Hu**, D. Chen and Y. Shi, "The importance of resource awareness in artificial intelligence for healthcare," *Nature Machine Intelligence*, 2023, pp. 1–12.

[J26] R. Zhang, C. Tang, X. Sun, M. Li*, W.Jin, P. Li, X. Cheng and **X. Hu**, "Sky-TCAM: Low-power skyrmion-based ternary content addressable memory," *IEEE Transactions on Electronic Devices (IEEE TED)*, Vol. 70, No. 7, 2023, pp. 3517–3522.

[J27] B. Wu, D. Reis, Z. Wang, Y. Wang, K. Chen, W. Liu, F. Lombardi and **X. Hu** , "An energy-efficient computing-in-memory (CiM) scheme using field-free spin orbit torque (SOT) magnetic RAMs," *IEEE Transactions on Emerging Topics in Computing (IEEE TETC)*, Vol. 11, No. 2, 2023, pp. 331–342.

[J28] G. Cauwenberghs, J. Cong, **X. Hu**[+], S. Joshi, S. Mitra, W. Porod and H.-S. P. Wong, "Micro/nano circuits and systems design and design automation: challenges and opportunities" *Proceedings of the IEEE*, Vol. 111, No. 6, 2023, pp. 561–574.

[J29] M. Yang, Q. Lou, R. Rajaei, M. R. Jokar, J. Qiu, Y. Liu, A. Udupa, F. T. Chong, J. M. Dallesasse, M. Feng, L. L. Goddard, **X. Hu** and Y. Li, "A hybrid optical-electrical analog deep learning accelerator using incoherent optical signals," *ACM Journal on Emerging Technologies in Computing Systems (ACM JETC)*, Vol. 19, No. 2, Article 14, 2023, pp. 1–24.

[J30] L. Liu*, A.F. Laguna, R. Rajaei, M.M. Sharifi*, A. Kazemi, X. Yin, M. Niemier and **X. Hu**, "A reconfigurable FeFET content addressable memory For multi-state Hamming distance," *IEEE Transactions on Circuits and Systems I (IEEE TCAS I)*, Vol. 70, No. 6, 2023, pp. 2356–2369.

[J31] S. Narla, P. Kumar, A. F. Laguna, D. Reis, **X. Hu**, M. Niemier and A. Naeemi, "Design of a compact spin-orbit-torque based ternary content addressable memory," *IEEE Transactions on Electronic Devices (IEEE TED)*, Vol. 70, No. 2, 2023, pp. 506–513.

[J32] M. Li*, P. Wu, B. Zhou, J. Appenzeller and **X. Hu**, "Cross-coupled Gated tunneling diodes with unprecedented PVCRs enabling compact SRAM design—Part II: SRAM circuit," *IEEE Transactions on Electron Devices (IEEE TED)*, Vol. 69, No. 11, 2022, pp. 6085–6088.

[J33] P. Wu, M. Li*, B. Zhou, **X. Hu** and J. Appenzeller, "Cross-coupled Gated tunneling diodes with unprecedented PVCRs enabling compact SRAM design—Part I: Device concept," *IEEE Transactions on Electron Devices (IEEE TED)*, Vol. 69, No. 11, 2022, pp. 6078–6084.

[J34] R. Mao, B. Wen, A. Kazemi*, Y.Zhao, A. F. Laguna*, R.Lin, N. Wong, M. Niemier, **X. Hu**, X. Sheng, C. E. Graves, J. P. Strachan and C. Li, "Experimentally validated memristive memory augmented neural network with efficient hashing and similarity search," *Nature Communications*, Vol. 13, No. 1, 2022, pp. 1–13.

[+] Corresponding author.

[J35] A. Kazemi*, F. Müller, M. M. Sharifi*, H. Errahmouni, G. Gerlach, T. Kämpfe, M. Imani, **X. Hu** and M. Niemier, "Achieving software-equivalent accuracy for hyperdimensional computing with ferroelectric-based in-memory computing," *Scientific Reports*, Vol. 12, 2022, Article No.: 19201.

[J36] S. Narla, P. Kumar, D. Reis∗, A. F. Laguna∗, M. Niemier, **X. Hu** and A. Naeemi, "Modeling and design for magnetoelectric ternary content addressable memory (TCAM)," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (IEEE JxCDC)*, Vol. 8, No. 1, 2022, pp. 44–52.

[J37] T. Wang, J. Zhou, L. Li, G. Zhang, K. Li and **X. Hu**, "Deadline and reliability aware multi-server configuration optimization for maximizing profit," *IEEE Transactions on Parallel and Distributed Systems (IEEE TPDS)*, Vol. 33, No. 12, 2022, pp. 3772–3786.

[J38] A. F. Laguna*, M.M. Sharifi*, A. Kazemi*, X. Yin*, M. Niemier and **X. Hu**, "Hardware-software co-design of an in-memory transformer network accelerator," *Frontiers in Electronics, Section Integrated Circuits and VLSI*, 2022, 3:847069.

[J39] S. Mishra*, D.Z. Chen and **X. Hu**, "Data-driven Deep supervision for medical image segmentation," *IEEE Transactions on Medical Imaging (IEEE TMI)*, Vol. 41, No. 6, 2022, pp. 1560–1574.

[J40] A. Kazemi*, M. M. Sharifi*, A. F. Laguna*, F. Müller, X. Yin, T. Kämpfe, M. Niemier and **X. Hu**, "FeFET multi-bit content-addressable memories for in-memory nearest neighbor search," *IEEE Transactions on Computers (IEEE TC)*, Vol. 71, No. 10, 2022, pp. 2565–2576.

[J41] D. Reis*, M. Niemier and **X. Hu**, ""IMCRYPTO: An in-memory computing fabric for AES encryption and decryption," *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 30, No. 5, 2022, pp. 553–565.

[J42] Q. Huang, D. Reis*, C. Li, D. Gao, M. T. Niemier, **X. Hu**, M. Imani, X. Yin and C. Zhuo, "Computing-in-emory using ferroelectrics: from single- to multi-input logic," Special Issue on Near-Memory and In-Memory Processing, *IEEE Design & Test of Computers*, Vol. 39, No. 2, 2022, pp. 56–64.

[J43] L. Zhang, S. Mishra*, T. Zhang*, Y. Zhang, D. Zhang, Y. Lv, M. Lv, N. Guan, **X. Hu**, D. Z. Chen and X. Han, "Design and assessment of convolutional neural network based methods for vitiligo diagnosis," *Frontiers in Medicine, section Dermatology*, 2021, 8:754202.

[J44] S. Mishra*, D. Z. Chen and **X. Hu**, "Image complexity guided network compression for biomedical image segmentation," *ACM Journal on Emerging Technologies in Computing Systems (ACM JETC)*, Vol. 18, No. 2, Article 26, 2021, pp. 1–23.

[J45] S. Mishra*, Y. Wang, C. Wei, D. Z. Chen and **X. Hu**, "VTG-Net: A CNN based vessel topology graph network for retinal artery/vein classification," *Frontiers in Medicine*, Vol. 8, 2021, pp. 2124 (10 pages).

[J46] D. Reis*, M. T. Niemier and **X. Hu**, "The implications of ferroelectric FET device models to the design of computing-in-memory architectures," Special Issue on Future Trends in Nanocomputing, *Journal of Integrated Circuits and Systems*, Vol. 16, No. 1, 2021, pp. 1–8.

[J47] T. Zhang*, T. Gong, S. Han, Q. Deng and **X. Hu**, "Fully distributed packet scheduling framework for handling disturbances in lossy real-time wireless networks," *IEEE Transactions on Mobile Computing (IEEE TMC)*, Vol. 20, No. 2, 2021, pp. 502–518.

[J48] B. Wu*, Z. Wang, Y. Li, Y. Wang, D. Liu, W. Zhao and **X. Hu**, "A NAND-SPIN based magnetic ADC," *IEEE Transactions on Circuits and Systems II: Express Briefs (IEEE TCAS II)*, Vol. 68, No. 2, 2021, pp. 617–621.

[J49] X. Xu, X. Zhang, B. Yu, **X. Hu**, C. Rowen, J. Hu and Y. Shi, "DAC-SDC low power object detection challenge for UAV applications," *IEEE Transactions on Pattern Analysis and Machine Intelligence (IEEE PAMI)*, Vol. 43, No. 2, 2021, pp. 392–403.

[J50] R. Rajaei*, M. M. Sharifi*, A. Kazemi*, M. Niemier and **X. Hu**, "Compact single-phase-search multi-state content addressable memory design using 1 FeFET/cell," *IEEE Transactions on Electron Devices (IEEE TED)*, Vol. 68, No. 1, 2021, pp. 109–117.

[J51] Y. Xi, H. Wu, B. Gao, J. Tang, A. Chen, M.-F. Chang, **X. Hu**, J. Van der Spiegel and H. Qian, "In-memory learning with analog resistive switching memory: a review and perspective," *Proceedings of the IEEE*, Vol. 109, No. 1, 2021, pp. 14–42.

[J52] P. Wu, D. Reis*, **X. Hu** and J. Appenzeller, "Two-dimensional transistors with reconfigurable polarities for secure circuits," *Nature Electronics*, Vol. 4, 2021, pp. 45–53.

[J53] L. Li, J. Zhou*, M. Chen, T. Wei and **X. Hu**, "Learning-based modeling and optimization for real-time system availability," Special Issue on Machine-Learning Architectures and Accelerators, *IEEE Transactions on Computers (IEEE TC)*, Vol. 70, No. 4, 2020, pp. 581–594.

[J54] W. Jiang, Q. Lou*, Z. Yan*, L.Yang, J. Hu, **X. Hu** and Y. Shi "Device-circuit-architecture co-exploration for computing-in-memory neural accelerators," *IEEE Transactions on Computers (IEEE TC)*, Vol. 70, No. 4, 2020, pp. 595–605.

[J55] D. Gao, D. Reis*, **X. Hu** and C. Zhuo, "Eva-CiM: a system-level performance and energy evaluation framework for computing-in-memory architectures," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 39, No. 12, pp. 5011–5024, 2020.

[J56] Y. Ding, W. Jiang, Q. Lou*, J. Liu, J. Xiong, **X. Hu**, X. Xu, and Y. Shi, "Hardware design and the competency awareness of a neural network," *Nature Electronics*, Vol. 3, 2020, pp. 514–523.

[J57] F. Molnàr, S.R. Kharel, **X. Hu** and Z. Toroczkai, "Accelerating a continuous-time analog SAT solver using GPUs," *Computer Physics Communications*, Vol. 256, 2020, 107469.

[J58] D.Y. Zhang, Y. Ma*, **X. Hu** and D. Wang, "Towards privacy-aware task allocation in social sensing based edge computing systems," *IEEE Internet of Things Journal (IEEE IoT-J)*, Vol. 7, No. 12, 2020, pp. 11384–11400.

[J59] B. Wu*, C. Wang, Z. Wang, Y. Wang, D. Zhang, D. Liu, Y. Zhang and **X. Hu**, "Field-free 3T2SOT MRAM for non-volatile cache memories," *IEEE Transactions on Circuits and Systems I (IEEE TCAS I)*, Vol. 67, No. 12, 2020, pp. 4660–4669.

[J60] D. Reis*, J. Takeshita, T. Jung, M. Niemier and **X. Hu**, "Computing-in-Memory for performance and energy efficient homomorphic encryption," *IEEE Transactions on VLSI Systems (IEEE TVLSI)*, Vol. 28, No. 11, 2020, pp. 2300–2313.

[J61] H. Wang , N. C. Audsley , **X. Hu** and W. Chang, "Meshed Bluetree: Time-predictable multi-memory interconnect for multi-core architectures," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 39, No. 11, 2020, pp. 3787-3798.

[J62] Y. Ma*, J. Zhou*, T. Chantem*, R. Dick, S. Wang and **X. Hu**, "Improving reliability of real-time embedded systems on integrated CPU and GPU platforms," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 39, No. 10, 2020, pp. 2218-2229.

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[I40] S. Hu, **X. Hu** and A. Zomaya, "Leveraging design automation techniques for cyber-physical system design," **Guest Editorial**, *IEEE Transactions on CAD of Integrated Circuits and Systems (IEEE TCAD)*, Vol. 35, No 5, 2016, pp. 697–698.

[I41] A. Chen, **X. Hu**, Y. Jin, M. Niemier and X. Yin*, "Enhancing hardware security with emerging transistor technologies," an **invited** paper, *ACM Great Lakes Symposium on VLSI (GLVLSI)* (ACM), May 2016, pp. 305–310.

[I42] R. Perricone*, **X. Hu**, J. Nahas, and M. Niemier, "Can beyond-CMOS devices illuminate dark silicon?" an **invited** paper, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2016, pp. 13–18.

[I43] A. Chen, **X. Hu**, Y. Jin, M. Niemier and X. Yin*, "Using emerging technologies for hardware security beyond PUFs," an **invited** paper, *Design Automation and Test in Europe (DATE)* (ACM/IEEE), March 2016, pp. 1544–1549.

[I44] M.T. Niemier and **X. Hu**, "Potential benefits from image processing hardware based on emerging transistor technologies," an **invited** paper, *International Society for Optics and Photonics (SPIE) Newsroom*, June 2015.

Grants and Sponsored Programs

Principal investigator of the following grants:

[G1] Microelectronics Commons, Department of Defense, *An Efficient Hardware Crypto Engine Based on In-Memory Computing*, $1,503,893.87, 11/15/2024 – 11/14/2025, (co-PI: Siddharth Joshi (ND), Michael Niemier (ND), Dayane Reis (USF), John Wallrabenstein (ADI) and Mike Burkland (RTX)).

[G2] Semiconductor Research Corporation (SRC), *Enabling Design Space Exploration of Monolithic-3D Logic and Memory Fabrics*, $391,500, 1/1/2023 – 12/31/2025, (co-PIs: Sung-Kyu Lim (Georgia Tech) and Michael Niemier (ND)).

[G3] AI Chip Center for Emerging Smart Systems Limited (ACCESS), *Physics-Based Compact Models and Physics-Informed AI Models for ReRAM and FeFETs*, $600,000, 9/14/2022 – 10/31/2024, (co-PI: Yiyu Shi (ND)).

[G4] DARPA, *Hardware and Programming Models Supporting In-memory Accelerators for Secure Information Processing*, $430,133, 1/1/2021 – 9/30/23, (co-PIs: Jose Martinez (Cornell) and Michael Niemier (ND)).

[G5] NSF, *An Analog Hardware System for Solving Boolean Satisfiability*, Supplement to Grant No. CCF-01644368, $150,000, 5/5/2017 – 6/30/2023, (co-PI: Zoltan Toroczkai (ND)). (The grant has been reassigned to a Notre Dame colleague due to my NSF appointment.)

[G6] EMD Electronics, *Understanding the design space of compute-in-memory accelerators*, $135,802, 8/1/2022 – 12/31/2022.

[G7] NSF, *Collaborative Research: PPoSS: Planning: S3-IoT: Design and Deployment of Scalable, Secure, and Smart Mission-Critical IoT Systems*, $32,718 (Notre Dame portion), 10/1/2020 – 9/30/2022, (five other PIs from other universities).

[G8] NSF, *Challenges and Opportunities for Electronic Design Automation in the Next Decade*, $43,308, 9/1/2020 – 8/31/2021, (for organizing an invitation-only NSF workshop).

[G9] NSF, *A Uniform Modeling Framework for Cross-Layer Benchmarking of CMOS and Beyond-CMOS Devices*, Supplement to Grant No. CCF-1640081, $149,349, 7/28/2020 – 8/31/2021 (senior personnel: Michael Niemier (ND)).

[G10] Semiconductor Research Corporation, *A Uniform Modeling Framework for Cross-Layer Benchmarking of CMOS and Beyond-CMOS Device*, $149,986, 11/1/2018 – 9/30/2019, (co-PI: Michael Niemier (ND)).

[G11] NSF, *Fabrication of Boolean Satisfiability (SAT) Solver Chips*, Supplement to Grant No. CCF-1640081, $49,749, 7/25/2018 – 8/31/2020, (co-PI: Arijit Raychowdhury (Georgia Tech)).

[G12] Purdue University, *TMD FETs for secure circuits through polymorphic logic gates*, $90,000, 3/1/2018 – 7/31/2020. (Sub-award from Applied Research Institute (ARI), PI: Joerg Appenzeller (Purdue University).)

[G13] IBM, *Exploiting TrueNorth for Biomedical Image Analysis Applications Based on New Deep Neural Network Models*, $60,000 (plus a TrueNorth hardware system), 1/15/2017 – 1/14/2018, (3 other co-PIs).

[G14] NSF, *CRI: Infrastructure for Supporting Biomedical Application Algorithm, Runtime Development and Resource Management*, Grant No. CCF-1629914, $500,000, 8/1/2016 – 7/31/2019, (4 other co-PIs).

[G15] NSF, *An Analog Hardware System for Solving Boolean Satisfiability*, Grant No. CCF-01644368, $299,612, 7/15/2016 – 6/30/2022, (co-PI: Zoltan Toroczkai (ND)).

[G16] University of Minnesota, *Center for Spintronic Materials, Interfaces and Novel Architectures (C-SPIN)*, $137,000, 5/1/2016 – 10/31/2017. (Sub-award from the STARnet program, Semiconductor Research Corporation (SRC) and Defense Advanced Projects Agency (DARPA), PI: Jianping Wang (University of Minnesota).)

[G17] NSF, *Reliability Driven Resource Management of Multi-Core Real-Time Embedded Systems*, Grant No. CNS-1319904, $500,000, 10/01/2013 – 9/30/2017. (Collaborative research with co-PIs: Thidapat Chantem (Virginia Tech) and Robert Dick (University of Michigan).)

[G18] Sandia National Laboratory, *Algorithm-Architecture Codesign for Exascale Computing*, Grant No. 1644261, $60,000, 1/8/2016 – 9/30/2016.

[G19] Sandia National Laboratory, *Algorithm-Architecture Codesign for Exascale Computing*, Grant No. 1524188, $60,000, 12/9/2014 – 9/30/2015.

[G20] Sandia National Laboratory, *Algorithm-Architecture Codesign for Exascale Computing*, Grant No. 1228867, $306,737, 4/19/2012 – 9/30/2014, (co-PIs: Danny Z. Chen (ND) and Mike Niemier (ND)).

[G21] Sandia National Laboratory, *Codesign for Exascale Computing*, Grant No. 1110893, $75,000, 4/01/2011 – 9/30/2011, (co-PIs: Danny Z. Chen (ND) and Mike Niemier (ND)).

[G22] University of Michigan, *Temperature-Aware Design for Real-time Applications*, Grant No. 3001661473, $38,888, 5/15/2010 – 4/30/2012. (Sub-award from NSF Grant No. CCF-0702761, PI: Robert Dick (University of Michigan).)

[G23] NSF, *Reconfiguration and Defect Tolerance in Quantum-dot Cellular Automata Based Nano-Devices*, Grant No. CCF-0702705, $275,000, 9/1/2007 – 8/31/2010, (co-PI: Marya Lieberman a(ND) nd Wolfgang Porod (ND)).

[G24] Prowess, Inc., *Development of an FPGA Based System for Accelerating Radiation Dose Calculation*, $85,567, 11/1/2006 – 2/28/2008, (co-PI: Danny Z. Chen (ND)).

[G25] Notre Dame Faculty Research Program Award, *Programmable Hardware for Dose Calculation in Radiation Therapy*, $10,000, 4/01/2006 – 3/31/2008.

[G26] NSF, *Flexible Scheduling in Real-Time Control Systems with Uncertainty*, Grant No. CNS-0410771, $270,000, 9/15/2004 – 8/31/2007, extended to 8/31/2008, (co-PI: Michael Lemmon (ND)).

[G27] NSF, *System-Level Approaches to Reducing Energy Consumption in Real-Time Embedded Systems*, Grant No. CCR-0208992, $119,975, 9/1/2002 – 8/31/2005, (co-PI: Joerg Henkel (NEC) and Danny Z. (ND)).

[G28] NSF, REU supplement to CAREER Award, *Experimental Platform and User Interface Development*, Grant No. CCR-9701416-005-REU, $10,000, 7/30/2002 – 4/30/2003.

[G29] NSF, Faculty Early Career Development (**CAREER**) Award, *Performance Analysis and Tradeoff for System-Level Design Exploration of Real-Time Embedded Systems*, Grant No. MIP-9701416, $210,000, 5/1/1997 – 4/30/2001.

[G30] NSF, REU supplement to CAREER Award, *Graphical Interface Development for EvoC*, Grant No. MIP-9701416-002-REU, $5,000, 6/1/1998 – 12/31/1998.

[G31] NSF, *Architectural Design Exploration for Real-Time Embedded Systems*, Grant No. MIP-9796162, $151,177, 9/1/1996 – 8/31/1999.

[G32] DARPA (Defense Advanced Research Projects Agency), *Architectural Design Exploration for Embedded Systems*, Contract No. DABT63-97-C-0048, $169,354, 7/1/1997 – 6/30/1999, (co-PI: Garrison Greenwood (WMU)).

[G33] Hewlett-Packard Laboratories, *Hardware-Software Codesign Research*, $279,000, 5/1/1995 – 7/30/2000, (co-PI: Garrison Greenwood (WMU)).

Co-PI of the following grants:

[G34] AI Chip Center for Emerging Smart Systems Limited (ACCESS), *AI Enabled Modeling and Design Automation for Computing-in-Memory Systems Based on Emerging Devices*, $600,000, 9/14/2022 – 10/31/2024, (PI: Yiyu Shi (ND)).

[G35] NSF, *Collaborative Research: SHF: Medium: A Comprehensive Modeling Framework for Cross-LayerBenchmarking of In-Memory Computing Fabrics: From Devices to Applications*, Grant No. CISE-2212239, $921,514, 9/1/2022 – 8/31/2026, (PI: Mike Niemier (ND), co-PI:

Kai Ni (Rochester Institute of Technology)). (The grant has been reassigned to a Notre Dame colleague due to my NSF appointment.)

[G36] NSF, *IRES Track 1: Impact of Emerging Information Processing Technologies on Architectures andApplications — a U.S.–French Partnership*, Grant No. OISE-2153622, $300,000, 7/1/2022 – 6/30/2025, (PI: Mike Niemier (ND)). (The grant has been reassigned to a Notre Dame colleague due to my NSF appointment.)

[G37] NSF, *Phase 1 I/UCRC University of Notre Dame: Center for Alternative Sustainable and Intelligent Computing (ASIC)*, Grant No. CCF-1822099, $749,995, 9/15/2018 – 8/31/2023. (I am a co-Director at the Notre Dame site, PI and ND-site Director: Yiyu Shi (ND), 1 other co-PI). (The grant has been reassigned to a Notre Dame colleague due to my NSF appointment.)

[G38] EMD Electronics, *Non-volatile memory technologies for in-memory compute and neuromorphic applications*, $124,911, 6/1/2022 – 12/31/2022, (PI: Mike Niemier (ND), co-PI: Kai Ni (Rochester Institute of Technology)).

[G39] Semiconductor Research Corporation, *Novel Devices and Circuits for Side Channels*, $150,000, 6/1/2018 – 5/31/2020, extended to 5/31/2021, (PI: Mike Niemier (ND), 3 other co-PIs).

[G40] NSF, *E2CDA:Type I: Extremely Energy Efficient Collective Electronics (EXCEL)*, Grant No. CCF-1640081, $2,646,150, 9/1/2016 – 8/31/2020. (I am a Thrust Lead, PI: Suman Datta (ND), 3 other co-PIs).

[G41] Semiconductor Research Corporation (SRC) and Defense Advanced Projects Agency (DARPA), *Center for Low Energy Systems Technology*, $29,860,355, 01/15/2013 – 10/31/2017, (PI: Alan Seabaugh (ND), and 26 other co-PIs).

[G42] NSF, *IRES: U.S.-Hungary Research Experience for Students on Non-Boolean Computer Architectures*, Grant No. IIA-1358072, $238,847, 9/1/2014 – 8/31/2017, (PI: Mike Niemier (ND), co-PIs: Wolfgang Porod (ND) and James Schmiedeler (ND)).

[G43] NSF, *NEB: Physics-Inspired Non-Boolean Computation based on Spatial-Temporal Wave Excitations*, Grant No. CCF-1124850, $1,600,000, 9/1/2011 – 8/31/2015, (PI: Wolfgang Porod (ND), co-PIs: Gary Bernstein (ND) and Mike Niemier (ND)).

[G44] DARPA, *Nanomagnet Logic*, Grant No. HR0011-10-C-0161, $2,123,367, 9/28/2010 – 12/31/2012, (PI: Wolfgang Porod (ND), and 3 other co-PIs).

[G45] NSF, *MRI: Characterization of and I/O for Magnetic Logic Structures*, Grant No. 0923243, $658,070, 9/1/2009 – 8/31/2012, (PI: Gary Berstein (ND), co-PIs: Wolfgang Porod and Michael Niemier).

[G46] NSF, *Dynamically Managing the Real-time Fabric of a Wireless Sensor-Actuator Network*, Grant No. CPS-0931195, $525,000, 9/1/2009 – 8/31/2012 (extended to 8/31/2013), (PI: Michael Lemmon (ND)).

[G47] Department of Navy, *Radiation-Hard Nanomagnetic Logic with Electronic Input and Output*, Grant No. N00014-09-1-1202, $482,673, 9/1/2009 – 12/31/2010, (PI: Wolfgang Porod (ND), co-PIs: Mike Niemier (ND) and Gary Bernstein (ND)).

[G48] NSF, *Integrated Energy-Aware Resource Scheduling for Wireless Real-Time Systems*, Grant No. CNS-0834180, $221,156, 9/15/2008 – 8/31/2010, (PI: Christian Poellabauer (ND)).

[G49] Semiconductor Research Corporation, *Midwest Institute for Nanoelectronics Discovery*, Phase 1, $3,100,000, 4/1/2008 – 3/31/2011. Phase 1.5, $2,200,986, 1/1/2011 – 12/31/2012, (PI: Alan Seabaugh (ND), and a number of other co-PIs).

[G50] Department of Defense, *Blending Processing into Advanced Memory Technologies to Enhance Massive, Memory-critical Applications*, $980,153, 3/4/2008 – 3/3/2010, (PI: Peter Kogge (ND), co-PIs: Jay Brockman (ND), Wolfgang Porod (ND), Michael Niemier (ND), Gary Berstein (ND)).

[G51] NSF, *Integrating Decentralized Control and Real-Time Scheduling for Networked Dynamical Systems*, Grant No. CCF-0720457, $160,000, 9/1/2007 – 8/31/2010, (PI: Michael Lemmon (ND)).

[G52] NSF, *Applications, Architectures, and Circuit Design for Nano-scale Magnetic Logic Devices*, Grant No. CCF-0621990, $300,000, 9/1/2006 – 8/31/2009, (PI: Michael Niemier (ND), co-PIs: Gary Bernstein (ND) and Wolfgang Porod (ND)).

[G53] NSF, *Ad Hoc Networks of Embedded Control Systems*, Grant No. ECS-0225265, $150,000, 10/1/2002 – 9/30/2005, (PI: Michael Lemmon (ND), co-PIs: Martin Haenggi (ND) and Panos Antsaklis (ND)).

[G54] NSF, *Performance Based Soft Real-Time Scheduling in Networked Control Systems*, Grant No. CCR-0208537, $160,000, 9/1/2002 – 8/31/2005, (PI: Michael Lemmon (ND), co-PIs: Panos Antsaklis (ND)).

[G55] NSF, *Geometric Problems in Radiosurgery, Radiation Therapy, and Other Medical Applications*, Grant No. CCR-9988468, $263,589, 5/1/2000 – 4/30/2003, (PI: Danny Z. Chen (ND)).
(Ranked No. 1 by the review panel among the proposals submitted to the respective area in 1999.)

[G56] Army Research Office, *Designing Efficient Search Operators for Constrained Optimization Problems*, $19,659, 9/22/1999 – 1/21/2000, (PI: Garrison Greenwood (WMU)).

Equipment (hardware and software) grants from industry:

[G57] Altera/AMD/Sun/XtremeData, XtremeData Development System, $15,300, 2006, (PI: Jay Brockman (ND)).

[G58] Xilinx, ISE Foundation and Embedded Development Kit license and 1 Virtex II FPGA board, $5,235, 2004.

[G59] Altera Corporation, 1 Stratix Pro board, $3,000, 2003.

[G60] Altera Corporation, FFT MegaCore Function license and associated hardware/software upgrades, $19,145, 2002.

[G61] Altera Corporation, 20 Quartus II software licensee and 1 Design Lab Package, $65,545, 2001.

[G62] Altera Corporation, 8 Excalibur-NIOS Development kits, $4,000, 2000.

Patents

[P1] **X. Hu**, Dayane Reis*, Michael T. Niemier and Haoran Geng*, "Circuits And Systems For Programmable In-Memory Encryption/Decryption Fabric Including RA/CAM Arrays For Parallel Processing Of Operations," U.S. Patent No. 12,470,364. Date of Issue: November 11, 2025.

[P2] X. Chen*, D. Z. Chen and **X. Hu**, *Methods of Operating a Graphics Processing Unit (GPU) to Train a Deep Neural Network Using a GPU Local Memory and Related Articles of Manufacture*, U.S. Patent No. 11,599,798. Date of Issue: March 7, 2023.

*Student or postdoctoral fellow advised or co-advised by X. Sharon Hu at the time of the patented work was confucted.

[P3] B. Sedighi*, **X. Hu**, M. T. Niemier and J. J. Nahas, *Systems and Methods for Filtering and Computation Using Tunneling Transistors*, U.S. Patent No. 9,825,132. Date of Issue: November 21, 2017. (Licensed by Semiconductor Research Corporation.)

[P4] B. Sedigh*, M. Niemier, **X. Hu** and I. Palit*, *Mixed Signal Processors*, U.S. Patent No. 9,712,146. Date of Issue: July 18, 2017. (Licensed by Semiconductor Research Corporation.)

[P5] B. Sedighi*, M. Niemier, **X. Hu** and J. J. Nahas, *Devices for Utilizing SymFETs for Low-Power Information Processing*, U.S. Patent No. 9,362,919. Date of Issue: June 7, 2016. (Licensed by Semiconductor Research Corporation.)

[P6] **X. Hu**, C.X. Yu, B. Zhou*, D.Z. Chen and K. Whitton*, *Methods and Apparatus for Hardware Based Radiation Dose Calculation*, U.S. Patent No. 8,494,115. Date of Issue: July 23, 2013. (Licensed by Prowess Inc., Chico, California, U.S.A.)

[P7] G. H. Bernstein, **X. Hu**, M. Niemier, W. Porod, M. T. Alam, and E. Varga, *Non-Majority MQCA Magnetic Logic Gates and Arrays Based on Misaligned Magnetic Islands*, U.S. Patent No. 8,058,906. Date of Issue: November 15, 2011.

[P8] D.Z Chen, **X. Hu**, S. Luan, C. Wang, X. Wu and C.X. Yu, *Error Control Algorithm for Step-and-Shoot Intensity Modulated Radiation Therapy*, U.S. Patent No. 7,466,797. Date of Issue: December 16, 2008.

[P9] S. Luan, D.Z Chen, **X. Hu**, C. Wang, X. Wu and C.X. Yu, *Segmentation Algorithmic Approach to Step-and-Shoot Intensity Modulated Radiation Therapy*, U.S. Patent No. US 7,283,611 B1. Date of Issue: October 16, 2007.

[P10] K. Ni, **X. Hu** and P. Ren*, *A Universal CAM Based on Write-Friendly BEOL Oxide Channel 2T0C DRAM for In-Memory Search with Frequent Update/*, U.S. Non-Provisional Application No. 119/639,603, April 6, 2026. *Pixel cell having a reset device with asymmetric conduction*, U.S. Patent Application Publication No. US20170048470A1, February 16, 2017.

Student Supervision

At University of Notre Dame:

Postdoctoral Fellows Supervised:

1. Mohamad Mehdi Sharifi, December 2024–June 2026, ArmanTek.
2. Zheyu Yan, December 2023–May 2024, Zhejiang University.
3. Dayane Reis, 2021–2022, University of South Florida.
4. Ramin Rajaie, 2018–2021. Jariet Technologies.
5. Indranil Palit, 2017–2018. Valeo North America (now at General Motors).
6. Xiaoming Chen, 2016–2017. Institute of Computing Technology, Chinese Academy of Sciences, China.
7. Chuancai Gu, 2016–2017. Northeastern University, China.
8. Maheshwar Sah, 2014–2015. Indiana University Purdue University, Fort Wayne, Indiana.
9. Behnam Sedighi, 2013–2014. Qualcomm.
10. Bo (Allen) Zhou, 2006–2008. Apple.

Ph.D. Theses Supervised or Co-Supervised (and Their First Full-Time Employer):

1. Liu Liu, Ph.D., August 2026, Nvidia.
2. Fu-Xiang Liang Ph.D., May 2026, Postdoctoral Fellow at University of Notre Dame.
3. Mohamad Mehdi Sharifi, Ph.D., December 2024, Postdoctoral Fellow at University of Notre Dame.
4. Mengyuan Li, Ph.D., May 2024. Apple.
5. Zheyu Yan, Ph.D., December 2023, Postdoctoral Fellow at University of Notre Dame.
6. Arman Kazemi, Ph.D., *Cross-Layer Design With Emerging Devices For Machine Learning Applications*, December, 2022, Amazon.
7. Ann Franchesca Laguna, Ph.D., *Accelerating Memory Intensive Algorithms and Applications Using In-Memory Computing*, May 2022, Assistant Professor at De La Salle University, Philippines.
8. Suraj Mishra, Ph.D., *Data-Driven Approaches for Biomedical Image Analysis*, May, 2022, Allen Institute for Cell Science.
9. Dayane Reis, Ph.D., *Circuits and Architectures for Data-Centric Computing*, December 2021, Postdoctoral Fellow, University of Notre Dame (currently Assistant Professor at University of South Florida).
10. Qiuwen Lou, Ph.D., *Cross-Layer Energy Efficient Hardware Design and Benchmarking with CMOS and Emerging Technologies*, May 2020, Amazon.
11. Xunzhao Yin, Ph.D., *Cross-Layer Integrated Design for Energy Efficient Computing*, August 2019, Assistant Professor, College of Information Science and Electronic Engineering, Zhejiang University, China.
12. Yue Ma, Ph.D., *Improving Reliability of Real-Time Embedded Systems*, December 2018. Apple.
13. Tianyu Zhang, Ph.D., supervised by Prof. Qingxu Deng at Northeastern University, China, *Real-Time Scheduling Research for Cyber-Physical Systems*, October 2018. Lecturer, Department of of Computer Science and Technology, Qingdao University, China (currently Assistant Professor at University of Iowa).
14. Robert Perricone, Ph.D., co-supervised by Prof. Michael Niemier, *Towards Computing in the Beyond-CMOS Era: A Study of Beyond-CMOS Circuits & Architectures*, May 2018. IBM.
15. Li Tang, Ph.D., *Performance and Energy Aware Workload Partitioning on Heterogeneous Platforms*, August 2017. Postdoctoral Fellow, Brookhaven National Laboratory (urrently staff Scientist at Los Alamos National Laboratory).
16. Indranil Palit, Ph.D., *Design and Evaluation of Circuits and Architectures based on Beyond-CMOS Device Technologies*, December 2016. Postdoctoral Fellow, University of Notre Dame (currently at GM).
17. Kai Xiao, Ph.D., *GPU-based Acceleration Techniques:Algorithms, Implementations, and Applications*, August 2015. Intel Labs (currently at Apple).
18. Shengyan Hong, Ph.D., *Real-Time Scheduling in Cyber-Physical Systems*, January 2015. Cadence (currently at Synopsys).
19. Shiliang (Shawn) Liu, Ph.D., *Design and Modeling for Nanomagnet Logic Circuits and Architectures*, August 2013. IBM (currently doing a startup).
20. Aaron Dingler, Ph.D., supervised by Prof. Michael Niemier, *Nanomagnet Logic: From Devices to Architectures*, May 2013. Tenure-track Assistant Professor, Department of

Engineering and Computer Science, Seattle Pacific University (currently a teaching faculty member at University of Notre Dame).

21. Steve Kurtz, Ph.D., supervised by Prof. Michael Niemier, *Nanomagnet Logic: Architectures, Design, and Benchmarking*, May 2013. IBM.
22. Michael Crocker, Ph.D., *Design, Fault Studies, and Performance Analysis for NML PLAs and Other NML Architectures*, August 2011. Tenure-track Assistant Professor, Department of Computer Science and Computer Engineering, Pacific Lutheran University.
23. Thidapat Chantem, Ph.D., *Real-time System Design Under Physical and Resource Constraints*, May 2011. Tenure-track Assistant Professor, Department of Electrical and Computer Engineering Department, Utah State University. (Currently Associate Professor at Virginia Tech.)
24. Zhong Wang, Ph.D., *Software Partitioning and Scheduling for Improving Performance and Energy Consumption*, May 2007. Synopsys.
25. Bren Mochocki, Ph.D., *The Impact of Dynamic Voltage and Frequency Scaling on the Energy Consumption, Schedulability and Predictability of Real-Time Embedded Systems*, December 2006. Epic Systems.
26. Yumin Zhang, Ph.D., *Low Power Design Techniques*, July 2002. Synopsys (currently at Google).
27. Gang Quan, Ph.D., *System Level Design Techniques for Real-Time Embedded Systems*, December 2001. Tenure-track Assistant Professor, Department of Computer Science and Engineering, University of South Carolina. Received the NSF CAREER Award in 2006. (Currently Full Professor at Florida International University.)
28. Lie-quan Lee, Ph.D., supervised by Andrew Lumsdaine, *Generic Programming for High-Performance Scientific Computing*, December 2002. Senior Software Developer, Stanford Linear Accelerator Center.

Postdoctoral Fellows and Ph.D. Students Currently being Supervised or Co-Supervised:

1. Fu-Xiang Liang, Postdoctoral Fellow, (started in June 2026).
2. Mohamad Mehdi Sharifi, Postdoctoral Fellow, (started in December 2024).
3. Jacob Bechtel, Ph.D. in progress (started in August 2025)
4. Naihao Xu, Ph.D. in progress (started in August 2025)
5. Pengyu Ren, Ph.D. in progress (started in August 2024)
6. Tomas Sousa Pereira, Ph.D. in progress (started in August 2024)
7. Ikenna Nwozo, Ph.D., in progress (started in August 2023).
8. Yifan Qin, Ph.D., in progress (started in August 2022).
9. Haoran Geng, Ph.D., in progress (started in January 2021).

Supervision of Selected Undergraduate Research Projects:

1. Biruk Molla, "AI, coding, and cutting metal to transcend stress," 08/25–present.
2. Ruibao Wang, "Hardware-software co-design for accelerating low-precision LLM," 03/2025–May 2026. (Remote advising, with the student being in Jilin University.)
3. Yi-Chun Liao, "In-memory retrieval for accelerating Retrieval Augmented Generation (RAG) models," 07/2025–1present. (Remote advising, with the student being in National Taiwan University.)

4. Seth Neu "AI, coding, and cutting metal to transcend stress," 08/25–12/2025.
5. Jianwen Wu, "Exploiting sparsity to accelerate neuro-symbolic AI reasoning," 08/2025–12/2025.
6. Shiyi Liu, "Design and analysis of analog content-addressable memories for tree-based machine learning algorithms," 08/2023–12/2023.
7. Che-Kai Liu, "Design and analysis of multi-level content-addressable memories," 07/2022–12/2022.
8. Drew Lair, "Accelerating deep reinforcement learning for embedded systems," 09/2022–12/2022.
9. Jonathan Abbott, "Accelerating deep reinforcement learning for embedded systems," 09/2021–5/2022.
10. Zephan Enciso, "Machine learning methods for circuit fault detection," 05/2020–08/2020.
11. John Joyce, "Circuit design with controllable gate transistors," 01/2016–12/2017.
12. Katherine Sanders, "Stochastic computing and nanomagnet logic (NML)," 06/2014–8/2015.
13. Arsal Habib, "Design and Evaluation of CNN-Based Circuits Using Beyond-CMOS Devices," summer 2014.
14. Bo Feng, "Exploiting the Power of GPU as Hardware Accelerators," summer 2014.
15. Yining Zhu, "Stochastic computing and nanomagnet logic (NML)," summer 2014.
16. Gina Andrews, "Exploring the Parameter Space of the Shape-Based MTJ Design for Mageneto-Electrical Interface," 2013-2014.
17. Libo Chen, "Design and Evaluation of CNN-Based Circuits Using Beyond-CMOS Devices," summer 2013.
18. Yangming Chong, "Exploiting the Power of GPU as Hardware Accelerators," summer 2013.
19. Yang Liu, "Stochastic Computing with Nanomagnet Logic (NML)," summer 2013.
20. Xinyu He, "Applying Wave-Based Computing to Implement a PDE Solver on FPGA," 2012.
21. Fiona Edwards-Murphy, "Study of Power/Performance Characteristics of Nanomagnet-Based Circuits," 2012.
22. Kobena Ampofo, "Performance and Energy Tradeoff in Nanomagnetic Wires," 2010-2012.
23. Yu Su, "Implementing an Online Transmission Rate Adjustment Policy for Reducing Energying in Wireless Networks," 2011.
24. Evan Lent, "Performance and Energy Tradeoff in Nanomagnetic Wires," 2009-2010.
25. Marcus-Tor Strickland (Senior at Morehouse College, Atlanta, GA), "Investigation of Design Parameters for Magnetic Electric Interface," 2009. (Partially supported by the Minority Engineering Program at Notre Dame.)
26. Michael Garrison, "Study of Biaxial Anisotrophy of Magnetic QCA Devices," 2008-2009.
27. Leonard Giannone, "Design of Signal Propagation Structures in Magnetic QCA Circuits," 2008-2009.
28. Jorge Andres Vendries Algarin, "Simulation of Magnetic QCA Circuit Constructs," 2008.
29. Brent Gills, "FPGA-Based Hardware Design for Medical Applications," 2008.
30. Jeffrey Simmer, "Energy-Aware Scheduling for IEEE 801.11e Based Networked Embedded Systems," 2007-2008.

31. Joseph Shaw (Junior at Tri-State University, Angola, IN), "FPGA-based Design of a Ray Tracing Engine," summer, 2007.
32. Peter Nistler, "Magnetic QCA Circuit Design," 2007-present.
33. Jared Bulosan, "Design and Simulation of Low-Power Networked Real-Time Systems," 2007.
34. Dylan Brandtner, "FPGA-based System Development for Radiation Dose Calculation," 2006-2007.
35. Kathleen Otten, "Energy-Aware DVS Scheduling," 2006-2007.
36. Bryn Mohan, "Development and Simulation of Molecular QCA Circuits," 2006-2007.
37. Daniel Dostal, "Clocking Circuitry for Molecular QCA," 2006.
38. John Korecki, "Implementing RT-Linux on Intel Xscale 80200evb Board," 2005-2006.
39. Mark Palladino, "Reducing Energy Consumption in Caches," 2005-2006. Recipient of the 2005-2006 College of Engineering Slatt Undergraduate Research Fellowship, University of Notre Dame.
40. Michael Crocker, "Evaluating the Benefits of BCache Design," 2003-2004.
41. Soo-Chang No, "Extending Intel Xscale 80200 Board with a DC/DC Converter," 2003-2004.
42. Bernard Montufar, "Visual Representation of ExPERTS Scheduling and Simulation Software," 2002–2004.
43. Brianne McNicholas, "Porting eCOS to Intel Xscale 80200 Board," 2003-2004.
44. Matthew Ivers, "Java Programming for GUI to ExPERTS," 2004.
45. Brandon McGirr, "Porting eCOS to Intel Xscale 80200 Board," 2004.
46. Dominic Antonelli, "QCA Circuit Partitioning," 2003-2004.
47. David Saracino, "Voltage Scaling on the Intel Xscale 80200 for the ExPERTS Research Project,", 2002–2003.
48. Francis Santoso, "Implementing JPEG Algorithms on an Nios Processor Board,", 2001–2002.
49. Ronald Setia, "Development of I/O Routines on an ARM Processor board,", 1999–2000.
50. Nathan Huston, "EvoC Graphical Interface Design with Tcl/Tk," 1999.
51. Raymond Ricordati, "EvoC Graphical Interface Design with Tcl/Tk," 1999.
52. Patrick Mitsch, "EvoC Graphical Interface Design," 1998.

At Western Michigan University:

M.S. Theses Supervised:

1. Lyle Benson, *A Term-Rewriting System for CORDIC Processors*, M.S., April 1995. Smith Industries.
2. Karthike Ethirajan, *Evolutionary Co-Design*, M.S., April 1997. Qualcomm.
3. Rajeshkumar Sambandam, *Predicting Timing Behavior in Architectural Design Exploration of Real-Time Embedded Systems*, M.S., April 1997. Intel.

Professional Activities

Journal Editorship:

- Associate Editor, *IEEE Transactions on Circuits and Systems for Artificial Intelligence (IEEE TCAS-AI)*, 2024-present.

- Editor in Chief, *ACM Transactions on Design Automation of Electronic Systems (ACM TODAES)*, 2020–2024.
- Associate Editor, *IEEE Transactions on Computer Aided Design (IEEE TCAD)*, 2020–2021.
- Guest Editor, special issue on Architecture Advances Enabled by Emerging Technologies, *IEEE Design & Test*, 2017.
- Member of the Guest Editorial Board, special issue on Real-Time Aspects in Cyber-Physical Systems, *ACM Transactions on Cyber-Physical Systems (ACM TCPS)*, 2017.
- Member of Editorial Board, *IEEE Design & Test*, 2016–2020.
- Associate Editor, *ACM Transactions on Cyber-Physical Systems (ACM TCPS)*, 2016–2020.
- Associate Editor, *IET Cyber-Physical Systems: Theory & Applications* , 2016–2020.
- Member of the Guest Editorial Board, special issue on CAD for Cyberphysical Systems, *IEEE Transactions on Computer Aided Design (IEEE TCAD)*, 2015.
- Associate Editor, *ACM Transactions on Embedded Computing Systems (IEEE TECS)*, 2008-2014.
- Member of the Guest Editorial Board, special issue on Power-Aware Design for Embedded Systems, *IEEE Transactions on Industrial Informatics (IEEE TII)* , 2011.
- Associate Editor, *ACM Transactions on Design Automation of Electronic Systems (ACM TODAES)*, 2005–2010.
- Member of the Guest Editorial Board, special issue on Power-Aware Computing, *IEEE Transactions on Industrial Informatics (IEEE TII)*, 2009.
- Associate Editor, *IEEE Transactions on Very Large Scale Integration Systems (IEEE TVLSI)*, 2005–2007.
- Member of the Guest Editorial Board, special issue for selected papers from PARC'05, *International Journal of Embedded Systems*, 2006.
- Member of the Editorial Board, *International Journal of Embedded Systems*, 2004–2006.
- Guest Editor of a special issue on Hardware/Software Co-Design for DSP, *IEEE Signal Processing Magazine*, 2004.
- Guest Editor of a special issue on Hardware/Software Co-Design, *IEEE Computer Magazine*, 2003.

Conference/Workshop Chair or Advising/Steering/Organizing Committee Member:

- Award Chair, *Embedded Systems Week (ESWEEK)* (ACM/IEEE), 2026.
- Chair of Sponsor Coordination Committee, *Design Automation Conference (DAC)* (ACM/IEEE), 2025–present.
- Member of Steering Committee, *Embedded Systems Week (ESWEEK)* (ACM/IEEE), 2024-present.
- Member of Executive Committee, *Design Automation Conference (DAC)* (ACM/IEEE), 2019–present.
- General Chair, General Co-Chair, *Embedded Systems Week (ESWEEK)* (ACM/IEEE), 2023, 2022.

- Member of Advisory Committee *IEEE International Conference on Intelligent Technology and Embedded Systems (ICITES)*, (IEEE), 2021–2023.
- General Chair, *IEEE Real-Time Systems Symposium (RTSS)* (IEEE), 2020.
- Technical Program Committee Chair, *IEEE Real-Time Systems Symposium (RTSS)* (IEEE), 2019.
- Program Co-Chair, *Hardware Aware Learning for Medical Imaging and Computer Assisted Intervention (HAL-MICCAI)*, 2019.
- General Chair, Vice General Chair, Program Chair, *Design Automation Conference (DAC)* (ACM/IEEE), 2018, 2017, 2016.
- Co-Chair, *Workshop on Non-conventional Approaches to Hard Optimization (NAHO)*, sponsored by NSF, 2017.
- Panel Chair, *Embedded Systems Week (ESWEEK)* (ACM/IEEE), 2017.
- Member of Organizing Committee, *Future Chips Forum*, 2017, 2018, 2019.
- Co-Chair of the Technical Program Committee, *Design Automation Conference (DAC)* (ACM/IEEE), 2014, 2015.
- Tutorial Chair, *Embedded Systems Week (ESWEEK)* (ACM/IEEE), 2015, 2016.
- Publicity Chair (North America), *Embedded Systems Week (ESWEEK)* (ACM/IEEE), 2012, 2013.
- Member of the Steering Committee, *International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS)* (ACM/IEEE), 2004–present.
- Chair of the Hardware/Software Co-Design Track, *IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)*, 2011.
- Co-Chair of the Power-Aware Designs Track, *ACM Symposium on Applied Computing (SAC)*, 2010, 2011.
- Member of the Advising Committee, *IEEE International Workshop on Wireless Mesh and Ad Hoc Networks (WiMAN)*, 2007.
- Chair of Subcommittee on Power-Aware Computing, *IFIP International Conference on Embedded and Ubiquitous Computing (EUC)*, 2007.
- Tutorial Chair and Vice Chair Subcommittee on Embedded and Real-Time Systems, *Asia South Pacific Design Automation Conference (ASPDAC)*, 2005.
- Workshop Chair, *International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS)* (ACM/IEEE), 2004.
- Technical Program Co-Chair, *International Conference on ASIC (ASICON)* (IEEE), 2003.
- General Co-Chair, *International Symposium on Hardware-Software Co-Design (CODES)* (ACM/IEEE), 2002.
- Tutorial Chair, *International Conference on Compilers, Architecture and Synthesis for Embedded Systems (CASES)* (ACM/IEEE), 2002.
- Technical Program Co-Chair, *International Symposium on Hardware-Software Co-Design (CODES)* (ACM/IEEE), 2001.

Conference Technical Program Committee Member (selected):

- *Design Automation and Test in Europe (DATE)* (ACM/IEEE), 2021.
- *IEEE Real-Time Systems Symposium (RTSS)*, 2008, 2011–2013.
- *Design Automation Conference (DAC)* (ACM/IEEE), 2002, 2010, 2011.
- *International Conference on Hardware-Software Codesign and System Synthesis (CODES+ISSS)* (ACM/IEEE), 2004–2011.
- *IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS)*, 2010–2012.
- *International Workshop on Cyber-Physical Networking Systems (CPNS)*, 2011, 2012.
- *ACM/IEEE International Conference on Green Computing and Communications (GreenCom)*, 2010.
- *IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA)*, 2009, 2010, 2011.
- *International Conference on Compilers, Architecture and Synthesis for Embedded Systems (CASES)* (ACM/IEEE), 2004–2005, 2008, 2009.
- *International Workshop on Cyber-Physical Systems (WCPS)*, 2008, 2009.
- Hardware/Software Codesign Track at *IEEE Real-Time Systems Symposium (RTSS)*, 2004–2007.
- *ACM Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES)*, 2005
- *Design, Automation and Test in Europe Conference (DATE)* (ACM/IEEE), 2004, 2003, 2001.
- *Asia South Pacific Design Automation Conference (ASPDAC)* (ACM/IEEE), 2004.
- *International Conference on Hardware/Software Codesign (CODES)* (ACM/IEEE/IFIP), 2000–2003. Session Chair in 2000.
- *International Conference on Computer-Aided Design (ICCAD)* (ACM/IEEE), 2000–2002. Session Moderator, 2001–2002.
- *IEEE Asia Pacific Conference on Circuits and Systems (APCCAS)*, 2000.
- Member of the Best Paper Selection Committee for the Embedded Systems Track, *Design Automation Conference (DAC)* (ACM/IEEE), 2000.
- *Great Lakes Symposium on VLSI (GLVLSI)* (IEEE), 1997.
- *International Conference on Computer Design (ICCD)* (ACM/IEEE), 1995–1996.

Professional Society Activities:

- Member of the IEEE Fellow Search Committee, *Circuits and Systems Society (CASS), IEEE*, 2025.
- Member of the Phil Kaufman Award Committee for Distinguished Contributions to EDA, *Council of Electronic Design Automation (CEDA), IEEE*, 2024–present.
- Chair of the Design Automation Conference Under-40 Innovators Award Committee, 2022, 2023.
- Member of the Ernest S. Kuh Early Career Award Committee, *Council of Electronic Design Automation (CEDA), IEEE*, 2021, 2022, 2023.
- Chair of the IEEE Fellow Selection Committee, *Council of Electronic Design Automation (CEDA), IEEE*, 2020, 2021.

- Member of the IEEE Fellow Selection Committee, *Council of Electronic Design Automation (CEDA), IEEE*, 2017, 2019.
- Chair, Executive Committee, *ACM Special Interest Group on Design Automation (SIGDA)*, 2018–2021.
- Member of the Executive Committee, *IEEE Technical Committee on Real-Time Systems (TCRTS)*, Diversity Subcommittee, 2018–2019.
- Member of IPSJ/IEEE Computer Society Young Computer Researcher Award Committee, 2018-2019. (IPSJ is the Information Processing Society of Japan).
- Member of the Executive Committee, *IEEE Technical Committee on Cyber-Physical Systems (TC-CPS)*, Award Subcommittee, 2017-present.
- Vice Chair, Executive Committee, *ACM Special Interest Group on Design Automation (SIGDA)*, 2015–2018.
- Member of the Executive Committee, *IEEE Technical Committee on Real-Time Systems (TCRTS)*, Conference Subcommittee, 2013–2015.
- Secretary/Treasurer, Executive Committee, *ACM Special Interest Group on Embedded Systems (SIGBED)*, 2011–2013.

Service to Government

- Lead Author/Program Director, NSF Solicitation on Enabling Access to the Semiconductor Chip Ecosystem for Design, Fabrication, and Training (Chip Design Hub), 2023–2025. This is a $10 million program aiming to broaden participation in integrated circuit chip design beyond the small number of institutions currently engaged in these activities.

- Co-organizer, NSF Workshop on Processing-In-Memory Technology, 2021. This is an NSF sponsored workshop aiming to provide a forum for leading experts in the relevant research thrusts of Processing-In-Memory (PIM) technology to brainstorm the latest research progress and discuss their visions of the critical challenges that need to be addressed in the near future.

- Lead Co-Chair, NSF Semiconductor Working Group, 2024. This is the working group which stewards and implements NSF-wide investments that address fundamental and translational research for future semiconductors as well as semiconductor based devices and systems, and workforce development for microelectronics design and manufacturing.

- Steering Committee Member, NSF Workshop on Micro/Nano Circuits and Systems design and Design Automation: Challenges and Opportunities, 2020. This workshop is co-organized by the Program Director of the NSF's Micro and Nano-electronic Systems and Architectures program. The goal of the workshop is to generate a report to the government from the research community recommending future research directions in micro and nano-electronic systems and architectures.

- Panelist: Panels for the Design Automation for Micro and Nano-systems Program, NSF, 2003, 2016, 2017, 2019.

- Member of the Search Committee for the director of NSF Division of Computing and Communication Foundations, 2017.

- Invited attendee of Workshop on System-on-a-Chip Design for HPC sponsored by DOE, DOD, NSF, and NASA, August 26-27, 2014. A total of 26 prominent researchers were invited. The goal of the workshop was to develop a strategy for an open fabric that is targeted at SoC designs for high end computing applications. A final report was produced based on the presentations and discussions at the workshop.
- Invited attendee of the NSF Workshop on Future Directions of Computer System Research, March 25-26, 2010. 30 prominent researchers from the field of computer system research were invited. The outcome of this workshop was a report that outlines new research directions in the general area of Computer Systems.
- Panelist: Panel for the Cyber-Physical System Program, NSF, 2009.
- Panelist: CAREER Award Panel, NSF, 2004, 2006, 2009, 2011.
- Reviewer of research proposals, NSF, 1996, 1997, 1998.
- Invited attendee of the NSF Workshop on Computer-Aided System Design, Boulder, Colorado, April 2-3, 1995. About 20 experts from U.S. in the CAD and system design areas were invited to this workshop, in which an NSF report was developed to define a strategic position for NSF in supporting new theory and technology for computer-aided system design.

Other Notable Services

- Member of International Advisory Committee of Institute of Microelectronics, Peking University, March 2019–2021.
- Overseas Review Expert, Chinese Academy of Sciences, Beijing, China, March 2015–2022.
- Member of External Review Committee, Electrical and Computer Engineering Graduate Program, University of California, Riverside, California, December 2016.
- International affiliated member, European Network of Excellence on Embedded Systems Design, ARTIST2, September 2004–August 2008.
- Opponent on the Ph.D. thesis defense committee for Mr. Sorin Manolache, Department of Computer and Information Science, Linköping University, Sweden, December 2005.
- Reviewer of ARISTEIA II proposals for National University of Singapore, Singapore, 2003.
- Reviewer for European Design and Automation Association (EDAA) Outstanding Dissertation Award, 2003.
- Reviewer of a publication by NATO Advanced Study Institute on Hardware/Software Codesign, 1995.

Conference Tutorials and Mini Courses

- Embedded Systems Week (ESWEEK), *Hardware-Aware Compilation and Simulation for In-Memory Computing*, September 2025.
- International VLSI Symposium on Technology, Systems and Applications (VLSI TSA), *In-Memory Computing: Cross-Layer Design from Devices to Applications*, April 2024.

- International Conference on Computer-Aided Design (ICCAD) (ACM/IEEE), *Ferroelectric FET Technology and Applications: From Devices to Systems - Cross-Layer Evaluation*, November 2021.
- Asia and South Pacific Design Automation Conference (ASPDAC) (ACM/IEEE), *A Journey from Devices to Systems with FeFETs and NCFETs*, January 2020.
- Invited lecturer for the Dragon Star program (offering graduate courses in China by overseas professors), delivered a week-long course on *Low-Power Computing*, Institute of Computing Technology, Chinese Academy of Sciences, May 2012.
- IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), *Using Sensitivity-Analysis and Dynamic Voltage Scaling for Power and Energy Management*, April 2006.

Selected Keynote/Invited/Panel Presentations (since 2010)

1. Invited Speaker, EcoCloud Center and Institute of Electrical and Micro Engineering, Ecole polytechnique fédérale de Lausanne EPFL, Lausanne, Switzerland, *Cross-Layer Co-Design for Accelerating Large-Scale Search Using NVM-based In-Memory computing*, June 2026.
2. Invited Speaker, Department of Information Technology and Electrical Engineering, Swiss Federal Institute of Technology ETH, Zurich, Switzerland, *Cross-Layer Co-Design for Accelerating Large-Scale Search Using NVM-based In-Memory computing*, June 2026.
3. Invited Speaker, Research and Development Center, TSMC, Hsinchu, Taiwan, *Cross-Layer Design for Enhancing the Resilience of In-Memory Computing to Device Variations*, April 2026.
4. Invited Speaker, Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, *Opportunities and Challenges in Accelerating Large-Scale Search Using NVM-based In-Memory ComputingPromises*, April 2026.
5. Invited Speaker, Department of Computer Science and Information Engineering, National Cheng-Kung University, Tainan, Taiwan, *Opportunities and Challenges in Accelerating Large-Scale Search Using NVM-based In-Memory ComputingPromises*, April 2026.
6. Invited Speaker, Research Center for Information Technology, Academia Sinica, Taipei, Taiwan, *Opportunities and Challenges in Accelerating Large-Scale Search Using NVM-based In-Memory ComputingPromises*, March 2026.
7. Invited Speaker, Eclectic Workshop, University of Sydney, Sydney Australia, *In-Memory Computing for Accelerating Learning — from Transistors to Algorithms/Applications*, February 2026.
8. Invited Speaker, Workshop on Managing Specialized and Heterogeneous Architectures, Simons Institute, Berkeley, CA, *In-Memory Computing based Accelerators for Large-Scale Search*, November 2025.
9. Panelist, Embedded Systems Week Conference (ESWEEK), Taipei, Taiwan, *In-Memory Computing for Embedded Systems: A Hype or A Reality*, October 2025.
10. Invited Speaker, Multicore and multiprocessor SoC Forum, Megeve, France, *Challenges and Opportunities in Accelerating Large-Scale Search Using NVM-Based In-Memory Computing*, June 2025.

11. **Keynote Speaker**, Workshop on Large Language Model Acceleration using Processing-In-Memory Architectures, Raleigh, NC, *Enhancing the Resilience of In-Memory Computing to Device Variations*, October 2024.

12. Panelist, Embedded Systems Week Conference (ESWEEK), Raleigh, NC, *Celebrating 20 years of ESWEEK*, October 2024.

13. **Keynote Speaker**, Annual Technology Symposium on "Frontiers of AI Accelerators: Technologies, Circuits and Applications IV", Hong Kong, China, *Cross-Layer Design for Enhancing the Resilience of In-Memory Computing to Device Variations*, June 2024.

14. Invited Speaker, Department of Electronic and Computer Engineering , Hong Kong University of Science and Technology, Hong Kong, China, *Multi-Bit Content-Addressable Non-Volatile Memories*, June 2024.

15. Invited Speaker, Department of Electrical Engineering , National Taiwan University, Taiwan, *Energy-Efficient In-Memory Search with Content-Addressable Non-Volatile Memories*, April 2024.

16. Invited Speaker, Corporate Research Seminar, Taiwan Semiconductor Manufacturing Company (TSMC), Taiwan, *Energy-Efficient In-Memory Search with Content-Addressable Non-Volatile Memories*, April 2024.

17. Invited Speaker, IEEE Solid-state Circuits Direction Workshop on Non-Traditional Computing Paradigms with Emerging Technologies for Energy Efficiency, Virtual, *Energy-Efficient In-Memory Search with Content-Addressable Non-Volatile Memories*, November 2023.

18. Invited Speaker, International Conference on Computer-Aided Design (ICCAD), *Algorithm/Hardware Co-design for Few-Shot Learning at the Edge*, November 2023.

19. Panelist, Embedded Systems Week Conference: Diversity, Equity and Inclusion in Embedded Systems Research, *Career Perspectives in Academia vs. Industry*, September 2023.

20. Invited Speaker, Lyon Institute of Nanotechnology, Ecole Centrale de Lyon, Lyon, France, *In-Memory Computing: from Devices to Applications — A Cross-Layer Perspective with a Focus on Content Addressable Memories*, September 2023.

21. Invited Speaker, CEA-Leti, Grenoble, France, *In-Memory Computing: from Devices to Applications — A Cross-Layer Perspective with a Focus on Content Addressable Memories*, September 2023.

22. **Keynote Lecturer**, Annual Technology Symposium on "Frontiers of AI Accelerators: Technologies, Circuits and Applications III", Hong Kong, China, *Cross-Layer Design Space Exploration for In-Memory Computing Based Accelerators*, June 2023. (I had to deliver the lecture virtually due to a travel issue.)

23. Invited Speaker, IEEE Symposium on VLSI Technology and Circuits (VLSI Symposium), Forum on Compute Paradigms for Secured Microelectronics and Combinatorial Optimization, Kyoto, Japan, *In-Memory-Computing Based Accelerators for Secure Computing*, June 2023.

24. Invited Speaker, Design Automation and Test in Europe (DATE), Dresden, Germany, *Analytical Modeling Tools for Rapid and Accurate Design Space Explorations of Technology Driven Architectures*, April 2023.

25. Invited Speaker, Department of ECE, Rutgers University, New Jersey, *In-Memory Computing: from Devices to Applications — A Cross-Layer Perspective with a focus on Content Addressable Memories*, April 2023.

26. Invited Speaker, Samsung, Virtual, *In-Memory Computing with Associative Memories – A Cross-Layer Perspective*, December 2022.

27. Invited Speaker, IBM T.J. Watson Research Center, Virtual, *In-Memory-Computing Based Accelerators for Privacy-Preserving Computing*, November 2022.

28. **Keynote Speaker**, International Green and Sustainable Computing Conference (IGSC), Virtual, *In-Memory Computing for Maximizing Energy Efficiency*, October 2022.

29. Invited Speaker, Department of EE, Stanford University, California, *In-Memory Computing with Associative Memories – A Cross-Layer Perspective*, October 2022.

30. Panelist, DAC Early Career Workshop, *Proposal Writing*, July 2022.

31. **Distinguished Speaker**, IEEE Council of Electronic Design Automation (CEDA) Distinguished Speaker Luncheon at Design Automation Conference (DAC), *In-Memory Computing: from Devices to Applications? A Cross-Layer Perspective*, July 2022.

32. Panelist, SIA-SRC Webinar: Collaboration Towards Decadal Plan Goals: Advances and Challenges in Semiconductor Hardware, *Cross-Layer Design From Devices to Applications*, June 2022.

33. Invited Speaker, Department of ECE, Duke University, North Carolina, *In-Memory Computing with Associative Memories – A Cross-Layer Perspective*, May 2022.

34. Super-Panel Panelist, Mondays in Memory (MiM): An In-Memory Computing Webinar Series, *Cross-Layer Design for In-Memory Computing – From Devices to Applications*, May 2022.

35. Plenary Speaker, Mondays in Memory (MiM): An In-Memory Computing Webinar Series, *In-Memory Computing with Associative Memories – A Cross-Layer Perspective*, February 2022.

36. Invited Speaker, IEEE International Electron Devices Meeting (IEDM), *In-Memory Computing with Associative Memories – A Cross-Layer Perspective*, December 2021.

37. Invited Speaker, High-Tech Women in Science and Technology, *In-Memory Computing for Machine Learning and Security Applications*, November 2021.

38. Invited Speaker, Workshop on Accelerator Computer Aided Design (ACCAD), *Design Space Exploration for In-Memory Computing with Associative Memories*, November 2021.

39. Plenary Speaker, IEEE CEDA Distinguished Lecture, *In-Memory Computing with Associative Memories — a Cross-Layer perspective*, August 2021.

40. Plenary Speaker, Synopsys Academic Speaker series, *Cross-Layer Design for In-Memory Computing - From FeFET based circuits to Machine Learning and Beyond*, January 2021.

41. **Keynote Speaker**, CCF Design Automation Conference (CCF-DAC), *In-Memory Computing based on FeFETs for Machine Learning and Beyond*, August 2020.

42. Panelist, *Panel on How to Juggle Different Tasks at Your (Academic) Job*, ACM/IEEE Forum: Advancing Diversity in EDA, Dresden, Germany, March 2020. (Cancelled due to COVID-19.)

43. **Keynote Speaker**, IEEE Non-Volatile Memory Systems and Applications Symposium (NVMA), *In-Memory Computing for Machine Learning Applications and Beyond*, August 2019.

44. **Keynote Speaker**, IEEE/ACM International Symposium on Nanoscale Architectures (NanoArch), *Exploiting Ferroelectric FETs: From In-Memory Computing to Machine Learning and Beyond*, July 2019.

45. Moderator, Forum: Advancing Diversity in EDA, *Panel on Negotiating: Practical Strategies for Women and URM in Tech*, June 2019.

46. **Keynote Speaker**, Xinhai International Forum, Dalian, China, *A Cross-Layer Perspective for Energy Efficient Processing — From beyond-CMOS devices to deep learning*, May 2019.

47. **Keynote Speaker**, The 3rd ChinaDA Forum, Beijing, China, *Cross-Layer Design for CMOS and Beyond*, May 2019.

48. Plenary Speaker, IEEE CEDA Distinguished Lecture, College of Microelectronics, Fudan University, Shanghai, China, *Exploiting Ferroelectric FETs: From In-Memory Computing to Machine Learning and Beyond*, March 2019.

49. **Keynote Speaker**, Symposium IX: Design And Automation Of Circuits And Systems, China Semiconductor Technology International Conference (CSTIC), *Edging Computing for Intelligent Healthcare*, March 2019.

50. Plenary Speaker, IEEE CEDA Distinguished Lecture, Institute of Microelectronics, Peking University, Beijing, China, *Exploiting Ferroelectric FETs: From In-Memory Computing to Machine Learning and Beyond*, March 2019.

51. Invited Speaker, School of Computer Science and Engineering, University of New South Wales, Sydney, Australia, *Energy/Performance/Reliability-Driven Design and Resource Management*, January 2019.

52. Invited Speaker, Huada Empyrean Software Co, Beijing, China, *GPU for DNN Acceleration — Dealing with Memory Challenges*, December 2018.

53. Plenary Speaker, IEEE CEDA Distinguished Lecture, Department of Electronic and Computer Engineering , Hong Kong University of Science and Technology, Hong Kong, China, *A Cross-Layer Perspective for Energy Efficient Processing — From Beyond-CMOS Devices to Deep Learning*, November 2018.

54. Plenary Speaker, IEEE CEDA Distinguished Lecture, Department of Computer Science, Tsinghua University, Beijing, China, *A Cross-Layer Perspective for Energy Efficient Processing — From Beyond-CMOS Devices to Deep Learning*, November 2018.

55. **Keynote Speaker**, China Test Conference (CTC), *A Cross-Layer Perspective for Energy Efficient Processing — From beyond-CMOS devices to deep learning*, August 2018.

56. **Keynote Speaker**, Great Lakes Symposium on VLSI (GLSVLSI), *A Cross-Layer Perspective for Energy Efficient Processing — From Beyond-CMOS Devices to Deep Learning*, May 2018.

57. Invited Speaker, Department of Electrical and Computer Engineering, Stony Brook University, Stony Brook, New York, *Resource Management for Wireless Networked Control Systems*, April 2018.

58. Invited Speaker, Computing for National Security Department, Brookhaven National Laboratory, Upton, New York, *A Cross-Layer Perspective for Energy Efficient Processing — From Beyond-CMOS Devices to Deep Learning*, April 2018.

59. Invited Speaker, Design Automation and Test in Europe (DATE), *Exploiting Ferroelectric FETs: From Logic-in-Memory to Neural Networks and Beyond*, March 2018.

60. Panelist, Forum: Advancing Diversity in EDA, *Panel on Negotiating: Practical Strategies for Women and URM in Tech*, March 2018.

61. **Keynote Speaker**, Symposium IX: Design And Automation Of Circuits And Systems, China Semiconductor Technology International Conference (CSTIC), *Which Neural Networks are the "Best"? A Case Study of Architecture, Circuit and Technology Impact on the MNIST Dataset*, March 2018.

62. Invited Speaker, Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, *Exploiting Ferroelectric FETs: Faster and Cooler Non-Volatile Logic-In-Memory and Beyond*, December 2017.

63. Invited Speaker, Center for Embedded Computer Systems (CECS) Colloquium, University of California, Irvine, California, *Network Resource Management in Cyber-Physical Systems*, Nov 2017.

64. Invited Speaker, Department of Electrical Engineering & Computer Science, Syracuse University, Syracuse, NY, *Cellular Neural Network Friendly Convolutional Neural Networks (CNNs with CNNs!)*, June 2017.

65. Invited Speaker, Design Automation and Test in Europe (DATE), *Advanced Spintronic Memory and Logic for Non-Volatile Processors*, March 2017.

66. **Keynote Speaker**, Symposium IX: Circuit Design, Systems and Applications, China Semiconductor Technology International Conference (CSTIC), *Exploiting Ferroelectric FETs: Faster and Cooler Non-Volatile Logic-In-Memory and Beyond*, March 2017.

67. Invited Speaker, Department of Electrical and Computer Engineering, Carnegie Mellon University, Pittsburgh, PA, *Exploiting Beyond-CMOS Transistors for Spatial-Temporal Information Processing*, March 2017.

68. Invited Speaker, Department of Computer Science, University of New Mexico, Albuquerque, New Mexico, *PeaPaw: Performance and Energy Aware Workload Partitioning on Heterogeneous Platforms*, September 2016.

69. Invited Speaker, University of Michigan-Shanghai Jiao Tong University Joint Institute, Shanghai, China, *Exploiting Beyond-CMOS Transistors for Spatial-Temporal Information Processing*, July 2016.

70. Invited Speaker, 30th Anniversary Colloquium Series, Department of Computer Science and Engineering, University of Connecticut, Storrs, Connecticut, *Increasing System Reliability Through Resource Management*, March 2016.

71. Panelist, Workshop on Resource Awareness and Application Auto-tuning in Adaptive and heterogeneous computing (RES4ANT), Dresden, Germany, *Panel on Moore's Law Is Still Alive! So Why Resource Awareness?* March 2016.

72. Invited Speaker, Design Automation and Test in Europe (DATE), Dresden, Germany, *Using emerging technologies for hardware security beyond PUFs*, March 2016.

73. Invited Speaker, Distinguished Colloquium Series, Department of Electrical and Computer Engineering, University of Maryland, College Park, Maryland, *Resource Management in Cyber-Physical Systems*, October 2015.

74. Invited Speaker, Department of Computer Science, Technical University of Dortmund, Germany, *Resource Management in Cyber-Physical Systems*, October 2015.

75. Invited Speaker, Institute of Electrical Engineering, École Polytechnique Fédérale de Lausanne, Lausanne, Switzerland, *Exploiting Beyond-CMOS Transistors for Non von Neumann Architectures*, March 2015.

76. Invited Speaker, Department of Electrical and Computer Engineering, Arizona State University, Tempe, Arizona, *Exploiting Beyond-CMOS Transistors for Non von Neumann Architectures*, February 2015.

77. Invited Speaker, International Conference on Computer-Aided Design (ICCAD), *Cellular Neural Networks for Image Analysis Using Steep Slope Devices*, November 2014.

78. Invited Speaker, Department of Electrical Engineering, Korea Advanced Institute of Science and Engineering (KAIST), Daejeon, Korea *Exploiting Beyond-CMOS Transistors for Non von Neumann Architectures*, October 2014.

79. Invited Speaker, Design Automation and Test in Europe (DATE), Dresden, Germany, *Impact of Steep-Slope Transistors on Non-von Neumann Architectures: CNN Case Study*, March 2014.

80. Invited Speaker, Exascale Grand Challenge (XGC) Meeting, Sandia National Laboratories, Albuquerque, New Mexico, *Towards Energy Efficient Heterogeneous Computing via Co-Design*, January 2014.

81. Invited Speaker, NVIDIA, Westford, MA, *GPU as Accelerators: Performance and Energy Implications*, October 2013.

82. Invited Speaker, Department of Electrical and Computer Engineering, Boston University, Boston, MA, *Improving System Reliability Through Temperature-Aware Design*, October 2013.

83. Invited Speaker, International Symposium on Low Power Electronics and Design (ISLPED), *TFET-based Cellular Neural Network Architectures*, September 2013.

84. Invited Speaker, Faculty of Information Technology and Bionics, Pázmány Péter Catholic University, Budapest, Hungary, *Beyond-CMOS Transistors and Their Use in Cellular Nonlinear Neural Network*, June 2013.

85. Invited Speaker, Scalable Computer Architecture Department, Sandia National Laboratories, Albuquerque, New Mexico, *Improving System Reliability Through Temperature-Aware Design*, November 2012.

86. Invited Speaker, Department of Electronic and Computer Engineering, Hong Kong University of Science and Technology, Hong Kong, China, *Computing with Nanomagnets*, April 2012.

87. Invited Speaker, School of Computer Science and Engineering, University of New South Wales, Sydney, Australia, *Meeting End-to-End Deadlines in Distributed Real-Time Embedded Systems*, February 2012.

88. Panelist, Panel on Exposing Hidden Execution Costs, Salishan Conference on High-Speed Computing, Gleneden Beach, Oregon, *No Free Lunch, No Hidden Cost: How Can Co-Design Help?* April 2011.

89. Invited Speaker, ITRS Workshop on Emerging Spin and Carbon Based Emerging Logic Devices, *Nanomagnet Logic*, Sept. 2010.

90. **Keynote Speaker**, Custom, Commodity and Codesign Workshop, *Hardware/Software Co-Design for Embedded Systems: How It May Impact High Performance Computing*, August 2010.

91. Invited Speaker, Institute of Computer and Network Engineering, Technical University of Braunschweig, Germany, *System-Level Performance Considerations Under the Peak Temperature Constraint*, July 2010.

92. Invited Speaker, IBM China Research Laboratory, Beijing, China, *Resource Management in Wireless Real-Time Environments*, June 2010.

93. Invited Speaker, Computer, Computational, and Statistical Sciences Division, Los Alamos National Laboratory, Albuquerque, New Mexico, *An Overview of HW/SW Co-design for Embedded System – Is it relevant to high performance computing?*, March 2010.

Consulting Activities

- Consultant, Hewlett-Packard Laboratories, Bristol, England, June-August, 1995-1997.
  Responsible for analyzing and making recommendations regarding the architectural design of several products including a tape drive system and a multi-media handheld unit.

Professional Affiliations

- Fellow of the Association of Computing Machinery (ACM)
- Fellow of the Institute of Electrical and Electronics Engineers (IEEE)
- Member of the American Association for the Advancement of Science (AAAS)
- Member of the Association of American Engineering Education (ASEE)
- Member of Society of Women Engineers (SWE)